ME15N25/ME15N25-G

N- Channel 250V (D-S) MOSFET

GENERAL DESCRIPTION

The ME15N25 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application.

FEATURES

- $R_{DS(ON)} \leq 265m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

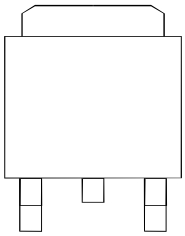
APPLICATIONS

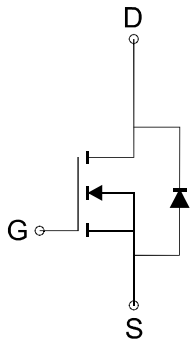
- DC/DC Converter
- Load Switch
- LCD/ LED Display inverter

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME15N25 (Pb-free)

ME15N25-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	250	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current*	Tc=25℃	I_D	17.1	A
	Tc=70℃		13.7	
Pulsed Drain Current		I_{DM}	68.6	A
Maximum Power Dissipation*	Tc=25℃	P_D	125	W
	Tc=70℃		80	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	1	℃/W

*The device mounted on $1in^2$ FR4 board with 2 oz copper

N- Channel 250V (D-S) MOSFET

Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	250			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2		4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=200V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 7A		220	265	mΩ
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.74	1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=200V, V_{GS}=10V, I_D=14A		70.8		nC
Qgs	Gate-Source Charge			16.2		
Qgd	Gate-Drain Charge			23.9		
Ciss	Input capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		3480		pF
Coss	Output Capacitance			112		
Crss	Reverse Transfer Capacitance			51		
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		2.3		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=125V, R_L =18Ω V_{GEN}=10V, R_G=25Ω		53		ns
t_r	Turn-On Rise Time			62.6		
$t_{d(off)}$	Turn-Off Delay Time			198		
t_f	Turn-On Fall Time			83.5		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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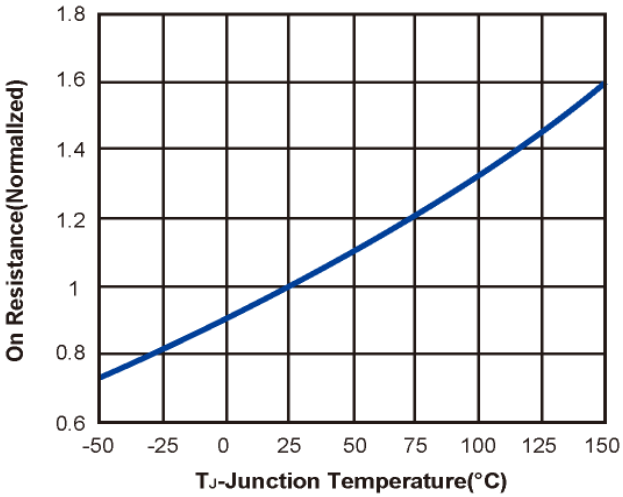
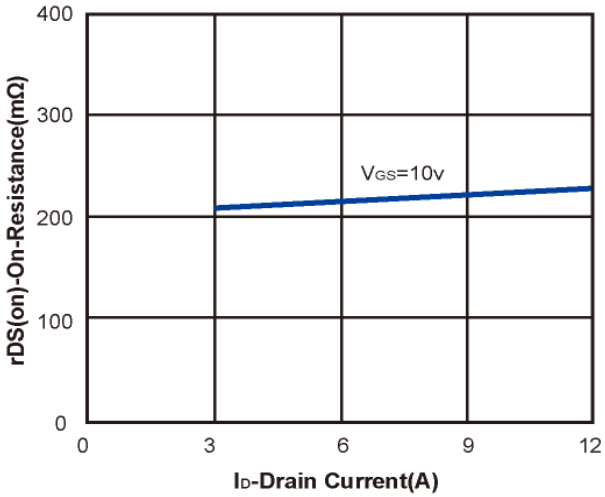
Typical Characteristics (T_J =25℃ Noted)

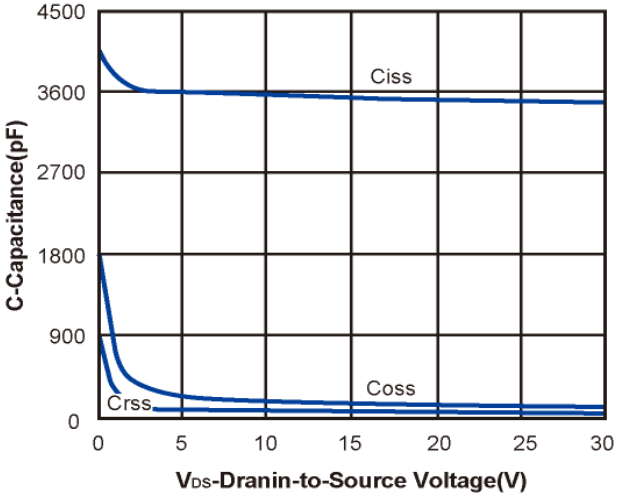
On Resistance vs. Junction Temperature



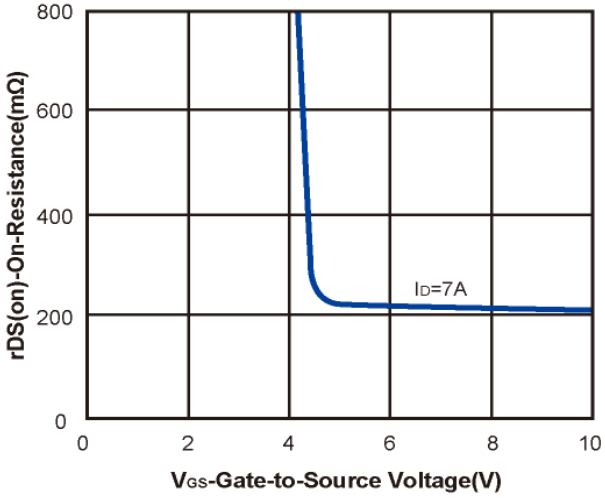
On Resistance vs. Drain Current



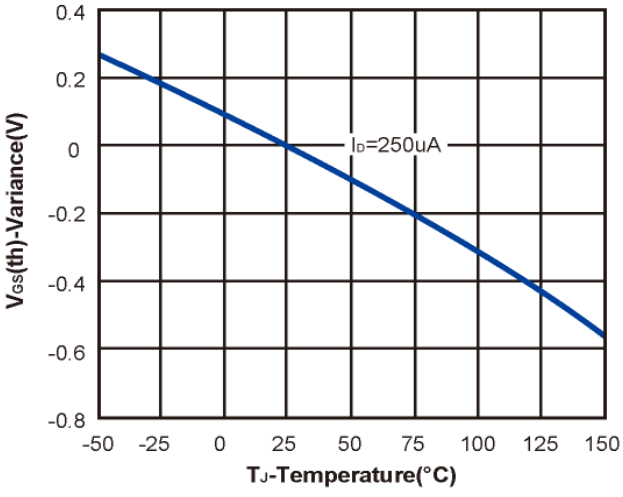
Capacitance



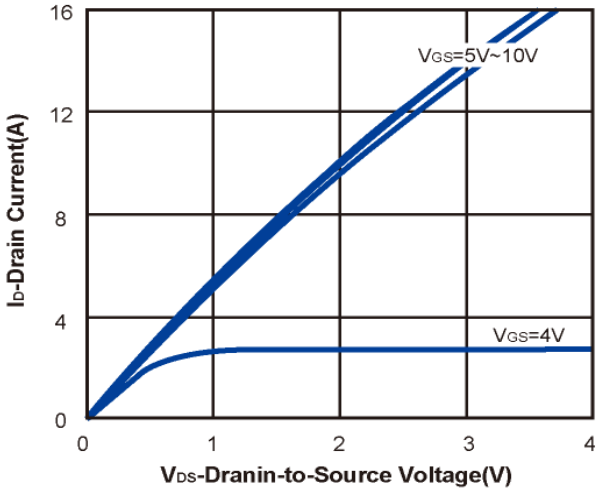
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



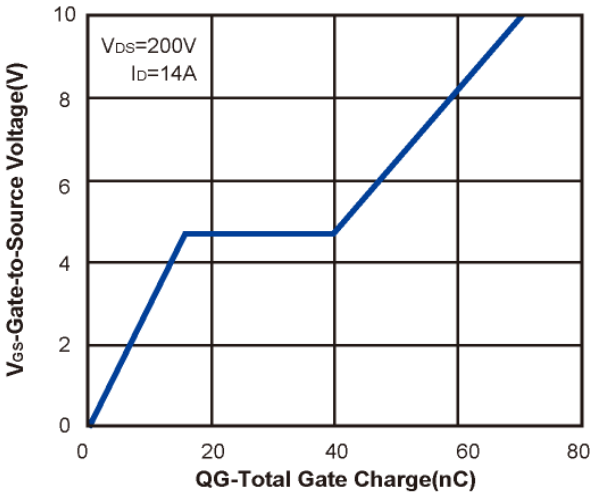
On-Region Characteristics



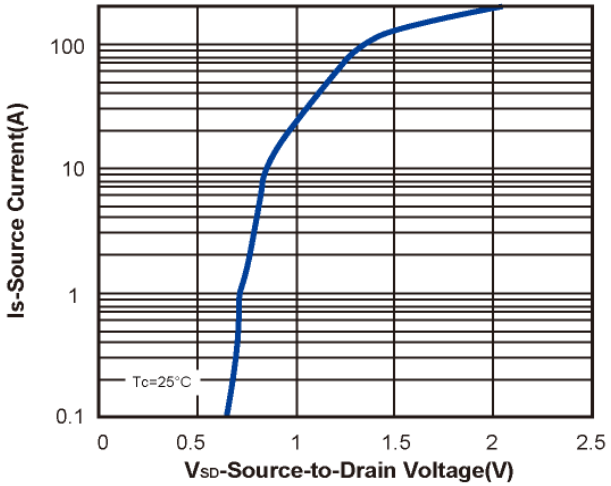
N- Channel 250V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

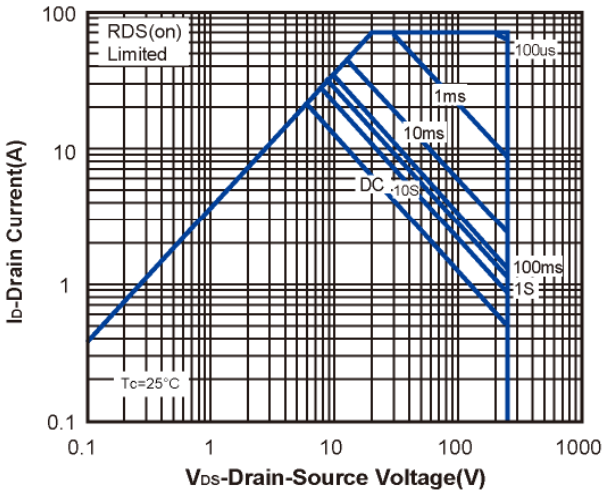
Gate Charge



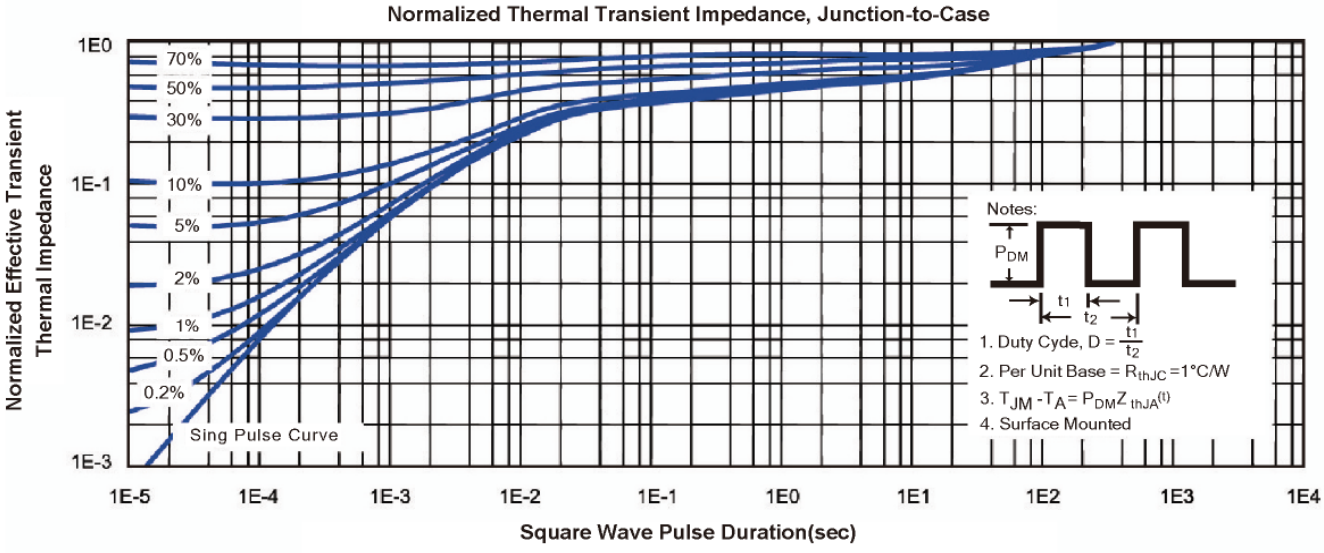
Body-diode characteristics



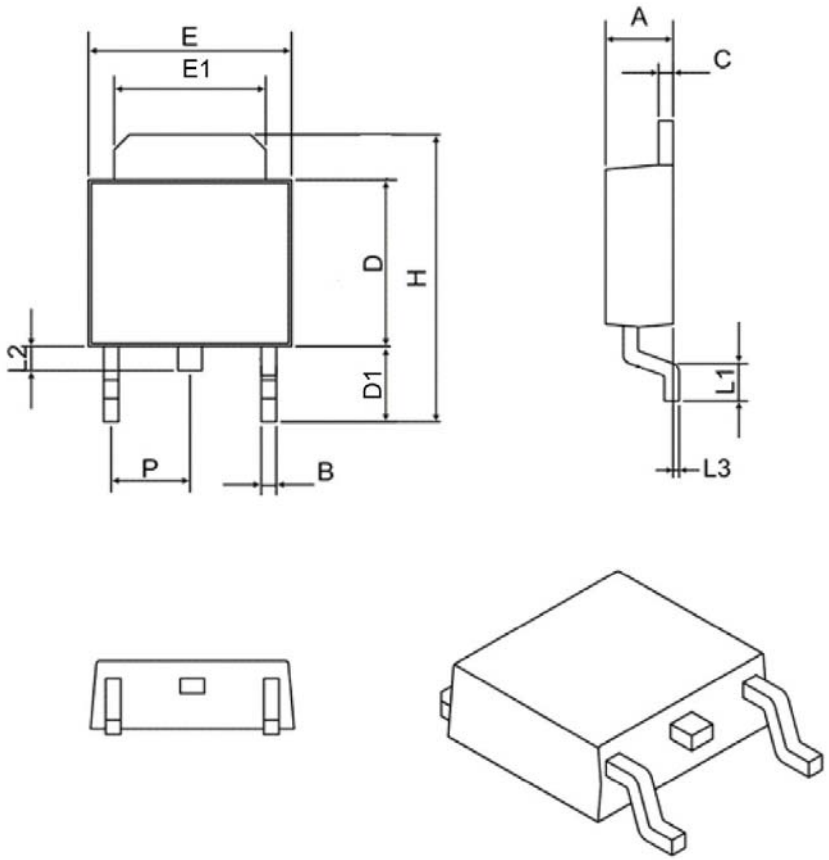
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	