

The S-8081B is a CMOS CR timer developed for appliances and industrial equipment use. It consists of a CR oscillator, a 20-stage divider, a power-on clear circuit, a trigger input chattering rejection circuit, an internal voltage regulator, a level shift circuit, and an output driver. It can be used as a high-precision, long-time monostable timer.

■ Features

- Wide power supply operating range : 4.5 to 16.5 V
- Low current consumption: 200 μ A max.(C = 200 k Ω ,
R = 0.0047 μ F, open output)
- Time can be set by external CR
- Excellent oscillation stability because of built-in voltage regulator
- Power-on clear circuit is integrated
- Both trigger I/O inverting operation and set/reset operation can be performed

■ Applications

- Time switch
- Long time delay generator

■ Pin Assignment

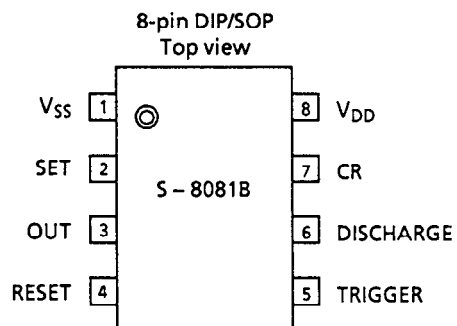


Figure 1

■ Block Diagram

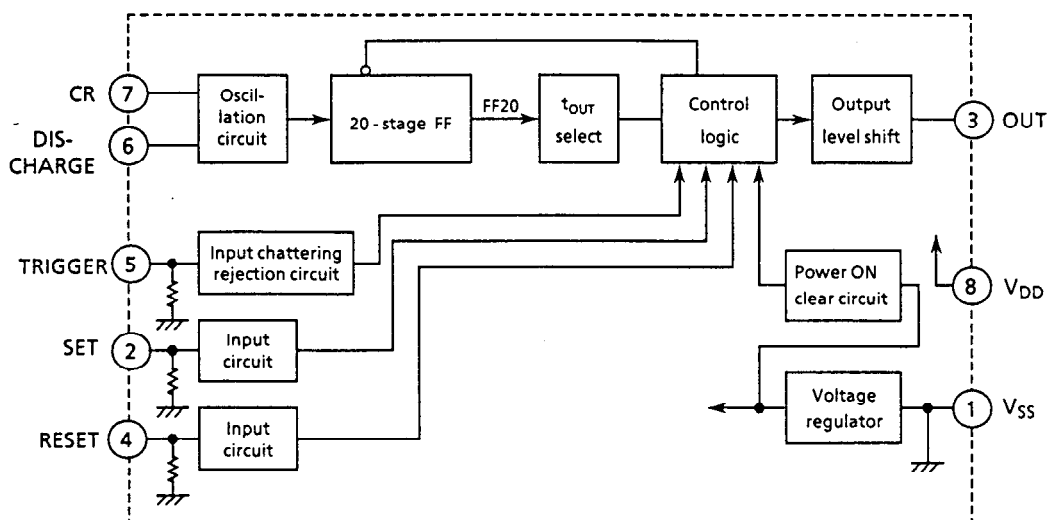


Figure 2

■ Timer Setting

The timer time t_{OUT} is decided by an external resistor R_T and an external capacitor C_T .

$$t_{OUT} = (K \times R_T \times C_T \times 2^{19}) \text{ sec.}$$

K = time constant coefficient

$10 \text{ s} \leq t_{OUT} \leq 10 \text{ hours}$ (recommended)

$R_T \geq 50 \text{ k}\Omega$, $C_T \geq 100 \text{ pF}$ (recommended)

Note : If other C_T or R_T is used than above recommended, the internal C and R influence t_{OUT} and it becomes different in each unit.

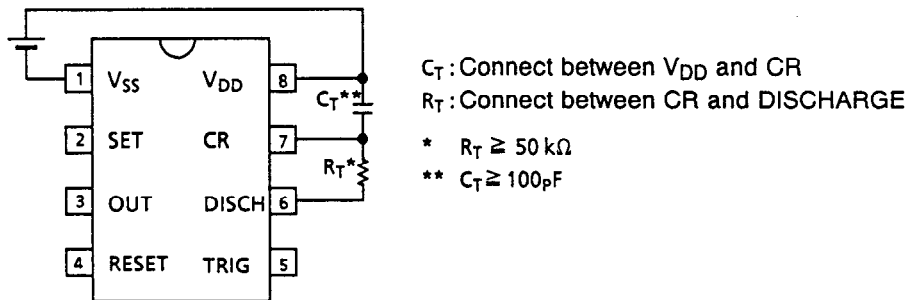


Figure 3 Connection of external C_T and R_T

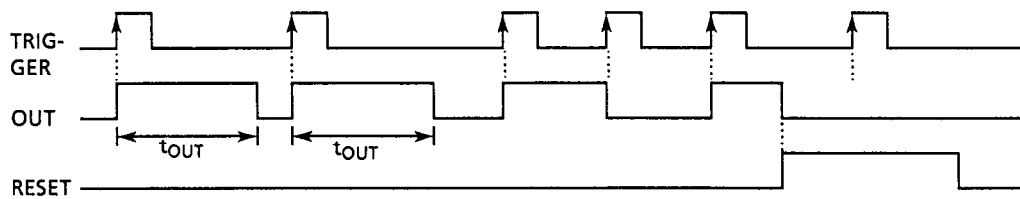


Figure 4 TRIGGER operation timing chart

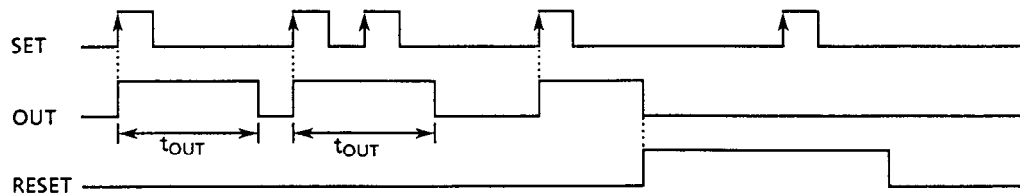


Figure 5 SET operation timing chart

$$t_{OUT} = t_{OSC} \times 2^{19}$$

$$t_{OSC} \approx K \times R_T \times C_T$$

(Recommended : $R_T \geq 50 \text{ k}\Omega$, $C_T \geq 100 \text{ pF}$)

■ Operation

1. SET terminal

At the rise of SET terminal, OUT goes high (V_{DD}) and frequency dividing operation starts.
This terminal has a pull-down resistor built in.

2. RESET terminal

By bringing RESET terminal high (V_{DD}), OUT goes low (V_{SS}) and the internal counter is reset.
Set or trigger input is ignored when reset is high.
This terminal has a pull-down resistor built in.

3. TRIGGER terminal

At the rise of TRIGGER terminal, OUT level is inverted. When OUT changes from low (V_{SS}) to high (V_{DD}), frequency dividing operation starts. When OUT changes from high (V_{DD}) to low (V_{SS}), the internal counter is reset. When starting TRIGGER operation during setting operation, reset the S-8081B before TRIGGER input. This terminal has a chattering rejection circuit and a pull-down resistor built in.

Chattering rejection time $\approx t_{osc} \times 7$

4. CR and DISCHARGE terminals

CR oscillation circuit can be constructed by connecting a timing capacitor C_T between V_{DD} and CR terminals, and by connecting a timing resistor R_T between CR and DISCHARGE terminals.

Set the oscillation period (t_{osc}) following the formula below.

$$t_{osc} \doteq K \times R_T \times C_T$$

K : time constant coefficient

5. OUT terminal

At the rise of SET or TRIGGER terminal, OUT goes high (V_{DD}) and frequency dividing operation starts. OUT goes low (V_{SS}) after $t_{osc} \times 2^{19}$.

When OUT is high (V_{DD}) if TRIGGER rises or RESET goes high (V_{DD}), OUT goes low (V_{SS}) and the internal counter is reset.

■ Absolute Maximum Ratings

Table 1

Unless otherwise specified: $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	$V_{SS} = 0\text{ V}$	18	V
Input/output voltage*	V_{IN}, V_{OUT}		$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}		- 30 to + 85	$^\circ\text{C}$
Storage temperature	T_{stg}		- 40 to + 125	$^\circ\text{C}$
Power dissipation	P_D	at 25°C	300	mW

* Excluding DISCHARGE terminal

■ Electrical Characteristics

Table 2

$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V}, T_a = 25^\circ\text{C}$

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage		V_{DD}		4.5	—	16.5	V
Operating current consumption		I_{DD}	$R = 200\text{ k}\Omega$ Open output $C = 0.0047\text{ }\mu\text{F}$	—	—	200	μA
SET, RESET, TRIGGER input pull-down resistance		R_{down}	$V_{IH} = V_{DD}$	50	—	400	$\text{k}\Omega$
High level input voltage		V_{IH}		$0.8 \times V_{DD}$	—	V_{DD}	V
Low level input voltage		V_{IL}		V_{SS}	—	$0.2 \times V_{DD}$	
High level output current		$ I_{OH} $	$V_{OH} = 5.7\text{ V}$ $V_{DD} = 8.0\text{ V}$	10	15	—	mA
Low level output current		$ I_{OL} $	$V_{OL} = 2.3\text{ V}$ $V_{DD} = 8.0\text{ V}$	20	30	—	
Low level output voltage		V_{OL}	$V_{DD} = 5.0\text{ V}$ $I_{OUT} = 3.2\text{ mA}$	—	—	0.4	V
Time constant coefficient		K	$C = 0.0047\text{ }\mu\text{F}$ $R = 200\text{ k}\Omega$	1.276	1.450	1.624	—
CR osc	Power supply voltage fluctuation*	$ \Delta f/f_{osc} $ $ \Delta V_{DD} $	$V_{DD} = 4.5$ to 16 V $C = 0.0047\text{ }\mu\text{F}$ $R = 200\text{ k}\Omega$	—	0.05	—	%/V
	Temperature fluctuation*	$ \Delta f/f_{osc} $ $ \Delta T $	$T_a = -20$ to $+60^\circ\text{C}$ $C = 0.0047\text{ }\mu\text{F}$ $R = 200\text{ k}\Omega$	—	0.10	—	%/ $^\circ\text{C}$

* Fluctuation of IC only

■ AC Electrical Characteristics

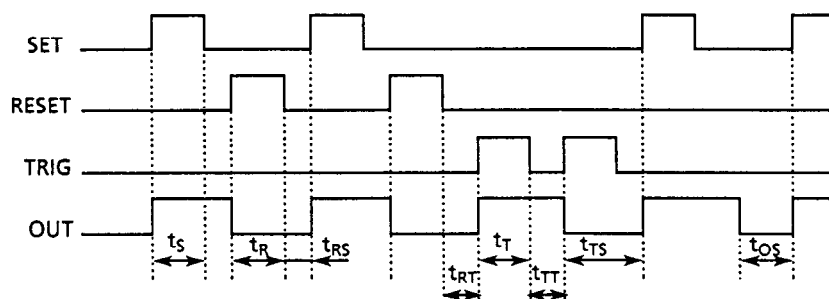
1. Input signal timing

Table 3

$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
SET pulse width	t_S	10	—	—	μs
RESET pulse width	t_R	10	—	—	μs
TRIG pulse width	t_T	$16 \times t_{osc}$	—	—	μs
RESET-SET pulse interval	t_{RS}	10	—	—	μs
RESET-TRIG pulse interval	t_{RT}	10	—	—	μs
TRIG pulse interval	t_{TT}	10	—	—	μs
SET input timing	t_{TS}	$t_T + 10$	—	—	μs
Pulse interval between timer operation finish and SET	t_{OS}	10	—	—	μs
Pulse interval between timer operation finish and TRIG	t_{OT}	10	—	—	μs

t_{osc} : oscillating frequency, ($t_{osc} = K \times R_T \times C_T$)



RESET input has the precedence over SET or TRIG input.

Figure 6

2. TRIG input pulse width and operation status

Table 4

$V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$

TRIG input pulse width	Operation
TRIG input pulse width $\geq 16 \times t_{osc}$	TRIG operation
$7 \times t_{osc} < \text{TRIG input pulse width} < 16 \times t_{osc}$	Indefinite*
TRIG input pulse width $\leq 7 \times t_{osc}$	No TRIG operation

*TRIG operation does not always start.

t_{osc} : oscillating frequency

■ Notes

1. Notes on operation

- Do not start TRIGGER operation during setting operation (see Figure 7). When starting TRIGGER operation during setting operation, reset the S-8081B before TRIGGER input.
- Do not set the RESET terminal high while SET or TRIGGER terminal is at high level. Or, the S-8081B will enter acceleration test mode. (see Figure 8)

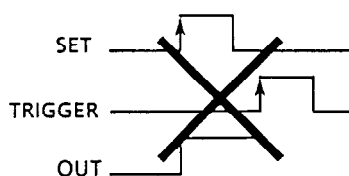


Figure 7

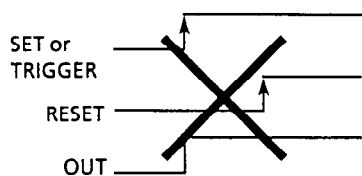


Figure 8

2. Status just after power-ON

A power-on clear circuit is built in the S-8081B and it initializes this IC at power-ON. During initialization, the S-8081B does not perform normal operation. Initialization time can not be defined clearly because it differs according to the voltage fluctuation at power-ON. See Table 5 for reference. Pay sufficient attention to the operation just after power-ON.

Table 5

Rise time	Initialization time*
< 1 ms	1 ms
≥ 1 ms	Time duration from power-ON to the time when V_{DD} reaches 4.5 V.

* Time duration from power-ON. At this time, the S-8081B does not operate normally.

3. CR oscillation

CR oscillation circuit is always operating while power supply voltage is applied.

4. V_{IH} level of input signal

When pulling up the SET, RESET or TRIGGER terminal, pay attention to V_{IH} level because they have pull-down resistors built in.

■ Acceleration Test Mode

The S-8081B has the acceleration test mode to check its F. F. function in a short time. This mode is performed as follows.

- (1) Put SET terminal from low to high level.
- (2) After (1), put RESET terminal from low to high level.
- (3) With keeping (1) and (2) status, input 511 clocks whose levels are the same as V_{DD} from CR terminal. (From 1st to 9th and from 11th to 19th stages of 20-stage F.F. are all high. The 20-stage F.F. starts operation at the falling of input signal.)
- (4) Put RESET terminal low.
- (5) Put SET terminal low.
- (6) Input 514th clock from CR terminal.
- (7) 20th stage of the 20-stage F.F. goes high from low, and the OUT terminal goes low.

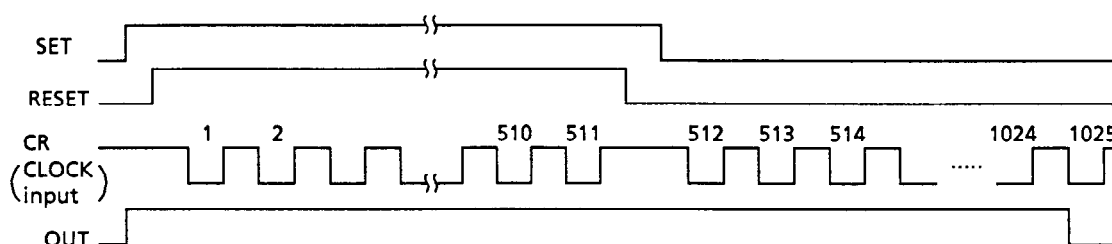


Figure 9

When releasing from acceleration test mode, initialize the S-8081B according to (a) or (b) below.

- (a) Turn the power off, and on again.
- (b) Put RESET terminal high level.

■ Dimensions

1. 8-pin DIP

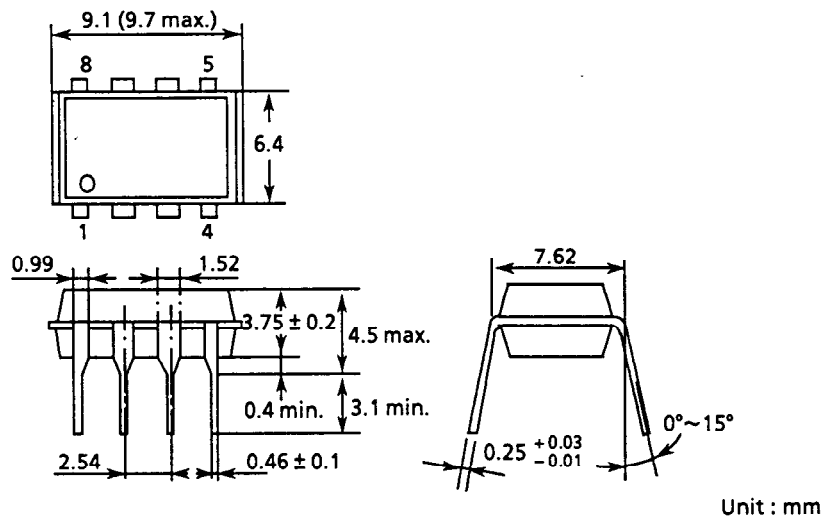


Figure 10

2. 8-pin SOP

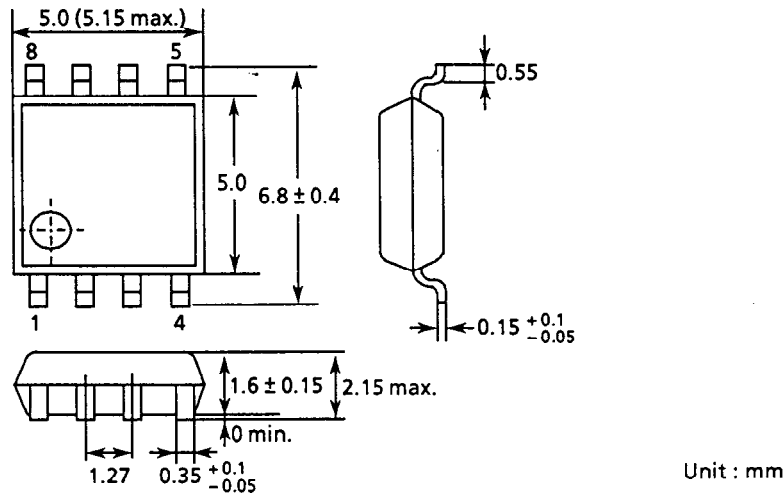


Figure 11

■ Application Circuit Example

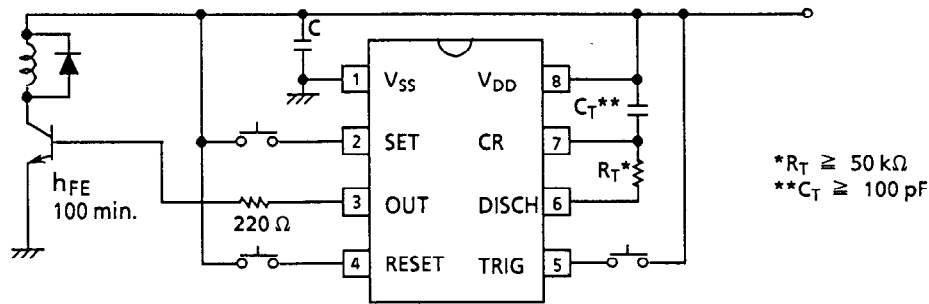
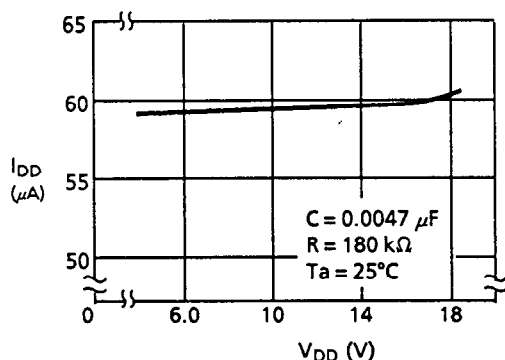


Figure 12

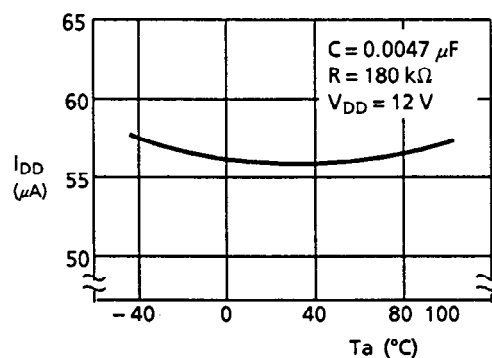
■ Characteristics

1. Current consumption characteristics

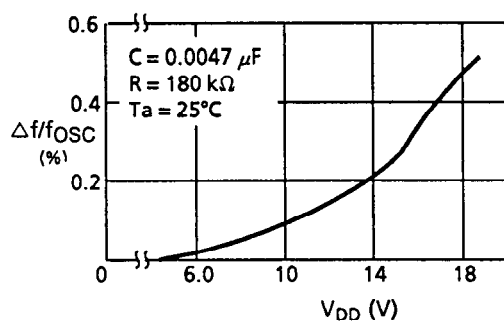
1.1 Operating current consumption I_{DD} – Power supply voltage V_{DD}



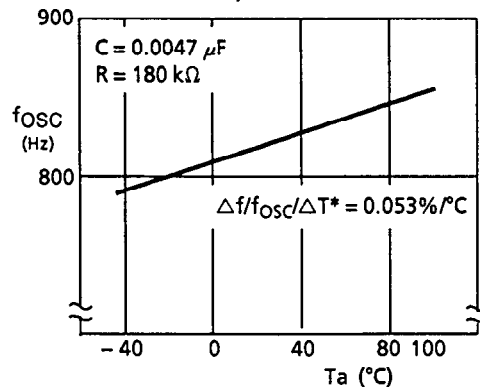
1.2 Operating current consumption I_{DD} – Ambient temperature T_a



2. Oscillation frequency $\Delta f/f_{OSC}$ – Power supply voltage V_{DD}

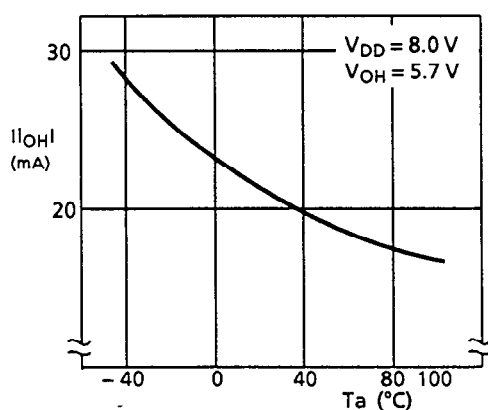


3. Oscillation frequency f_{OSC} – Ambient temperature T_a

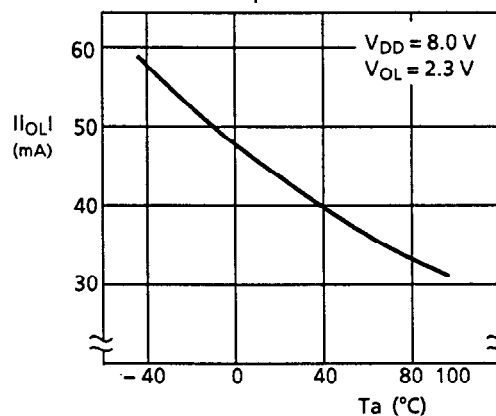


* $\Delta f/f_{OSC}/\Delta T$ is fluctuation of IC only.

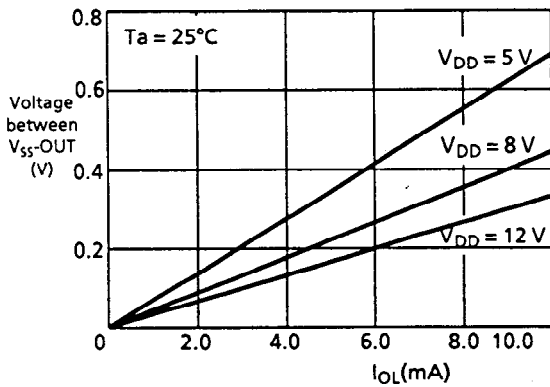
4. High level output current $|I_{OH}|$ – Ambient temperature T_a



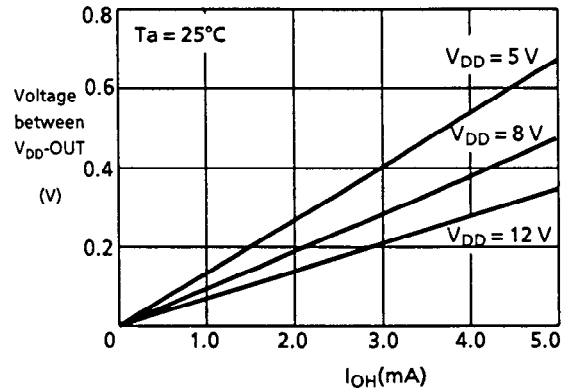
5. Low level output current $|I_{OL}|$ – Ambient temperature T_a



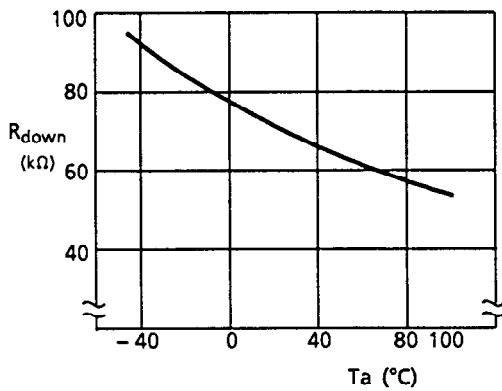
6. Output Nch driver characteristics



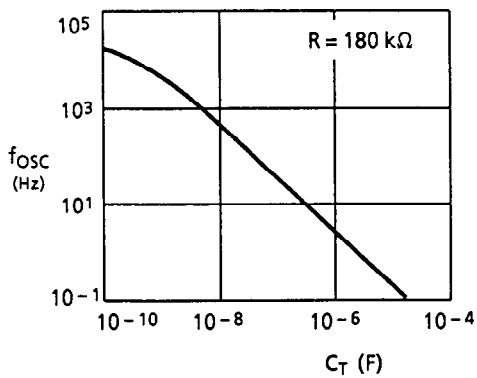
7. Output Pch driver characteristics



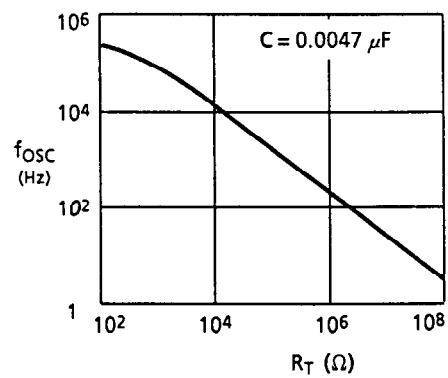
8. Pull-down resistance R_{down} - Ambient temperature T_a



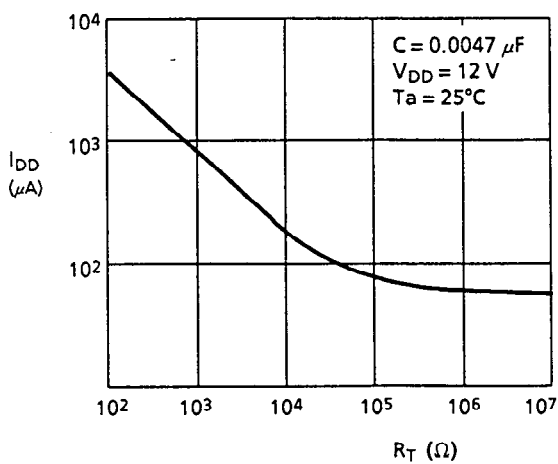
9. Oscillation frequency f_{OSC} - External capacitance C_T



10. Oscillation frequency f_{OSC} - External resistance R_T



11. Current consumption I_{DD} - External resistance R_T



12. Current consumption I_{DD} - External Capacitance C_T

