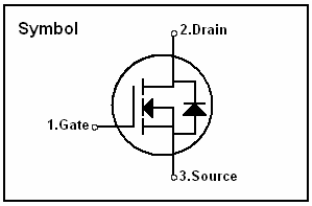
Truesemi

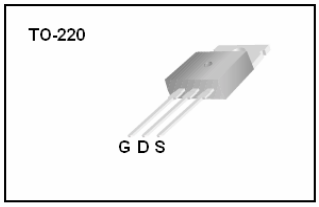
TSP8N60M/TSF8N60M

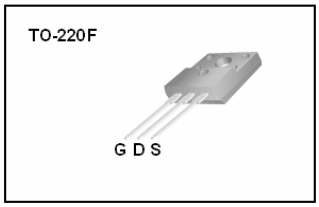
600V N-Channel MOSFET

Features

- 7.5A,600v,RDS(on)=1.2Ω@VGS=10V
- Gate charge (Typical 30nC)
- High ruggedness
- Fast switching
- 100% AvalancheTested
- Improved dv/dt capability







General Description

This Power MOSFET is produced using Truesemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. These devices are well suited for high efficiency switch mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Absolute Maximum Ratings

Symbol	Parameter		TSP8N60M	TSF8N60M	Units
VDSS	Drain to Source Voltage		600		V
ID	Continuous Drain Current(@TC = 25°C)		7.5	7.5*	A
	Continuous Drain Current(@TC = 100°C)		4.5	4.5*	A
IDM	Drain Current Pulsed	(Note 1)	30	30*	A
VGS	Gate to Source Voltage		±30		V
EAS	Single Pulsed Avalanche Energy	(Note 2)	285		mJ
EAR	Repetitive Avalanche Energy	(Note 1)	15.5		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5		V/ns
PD	Total Power Dissipation(@TC = 25 °C)		165	55	W
	Derating Factor above 25 °C		1.21	0.4	W/°C
TSTG, TJ	Operating Junction Temperature & Storage Temperature		-55 ~ 150		°C
TL	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300		°C

Thermal Characteristics

Symbol	Parameter	TSP8N60M	TSF8N60M	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.85	2.2	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ	0.5	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

Electrical Characteristics (TC = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	600	--	--	V
ΔBV_{DSS} /ΔT_J	Breakdown Voltage Temperature coefficient	I_D = 250uA, referenced to 25 °C	--	0.57	--	V/°C
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 600V, V_{GS} = 0V	--	--	10	uA
		V_{DS} = 480V, T_C = 125 °C	--	--	100	uA
I_{GSS}	Gate-Source Leakage, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
	Gate-source Leakage, Reverse	V_{GS} = -30V, V_{DS} = 0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	2.0	--	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-state Resistance	V_{GS} =10 V, I_D = 3.75A	--	1.0	1.2	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} =0 V, V_{DS} =25V, f = 1MHz	--	1255	--	pF
C_{oss}	Output Capacitance		--	115	--	
C_{rss}	Reverse Transfer Capacitance		--	14.2	--	
Dynamic Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} =300V, I_D =7.5A, R_G =25Ω (Note 4, 5)	--	22	--	ns
t_r	Rise Time		--	90	--	
$t_{d(off)}$	Turn-off Delay Time		--	76	--	
t_f	Fall Time		--	44	--	
Q_g	Total Gate Charge	V_{DS} =480V, V_{GS} =10V, I_D =7.5A (Note 4, 5)	--	30	--	nC
Q_{gs}	Gate-Source Charge		--	5.2	--	
Q_{gd}	Gate-Drain Charge(Miller Charge)		--	16.3	--	

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit.
I_S	Continuous Source Current	Integral Reverse p-n Junction	--	--	7.5	A
I_{SM}	Pulsed Source Current	Diode in the MOSFET	--	--	30	
V_{SD}	Diode Forward Voltage	I_S=7.5A, V_{GS} =0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=7.5A, V_{GS}=0V,dI_F/dt=100A/us	--	390	--	ns
Q_{rr}	Reverse Recovery Charge	I_S=7.5A, V_{GS}=0V,dI_F/dt=100A/us	--	3.3	--	uC

※ NOTES
1. Repeativity rating : pulse width limited by junction temperature
2. L = 20mH, I_{AS} =7.5A, V_{DD} = 50V, R_G = 50Ω , Starting T_J = 25°C
3. I_{SD} ≤ 7.5A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse Width ≤ 300us, Duty Cycle ≤ 2%
5. Essentially independent of operating temperature

Fig 1. On-State Characteristics

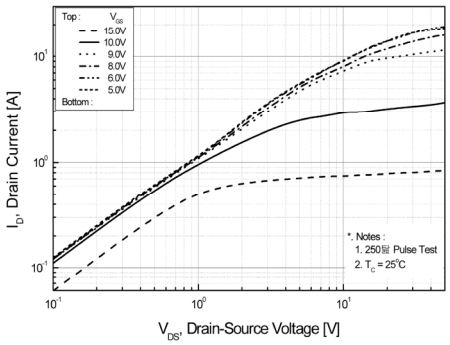


Fig 2. Transfer Characteristics

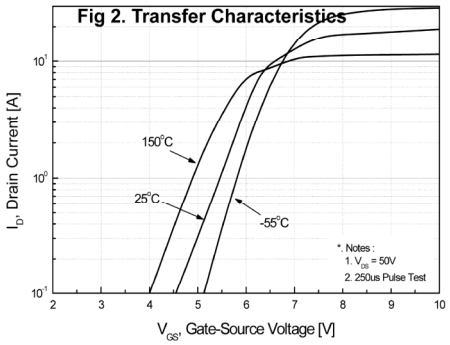


Fig 3. On Resistance Variation vs. Drain Current and Gate Voltage

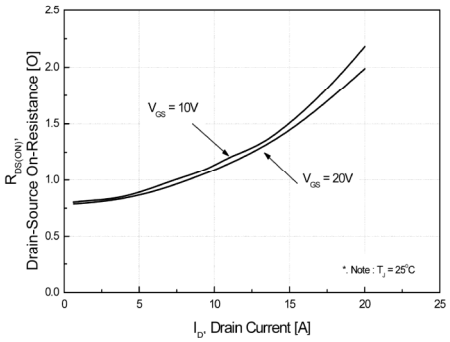


Fig 4. On State Current vs.

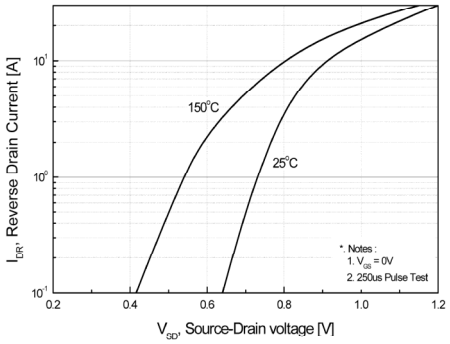


Fig 5. Capacitance Characteristics (Non-Repetitive)

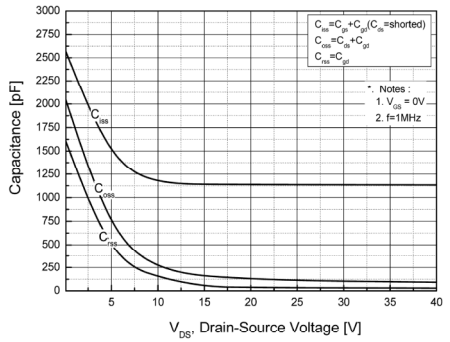


Fig 6. Gate Charge Characteristics

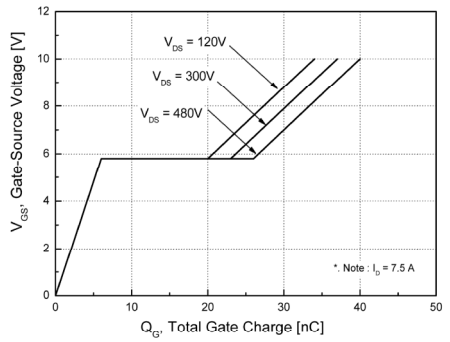


Fig 7. Breakdown Voltage Variation vs. Junction Temperature

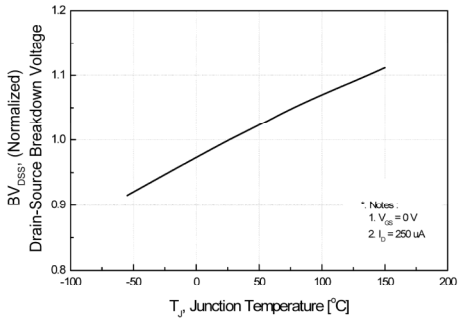


Fig 8. On-Resistance Variation vs. Junction Temperature

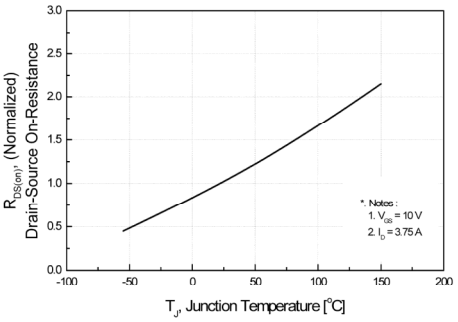


Fig 9-1. Maximum Safe Operating Area fo TSP8N60M

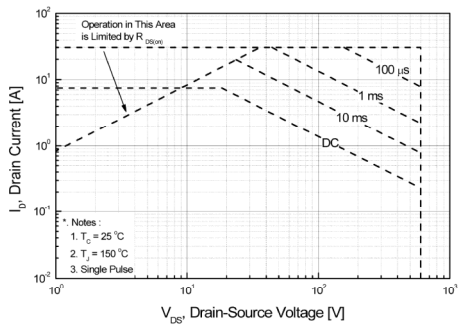


Fig 9-2. Maximum Safe Operating Area for TSF8N60M

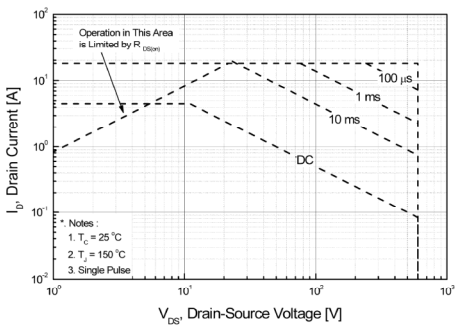


Fig 10. Maximum Drain Current vs. Case Temperature

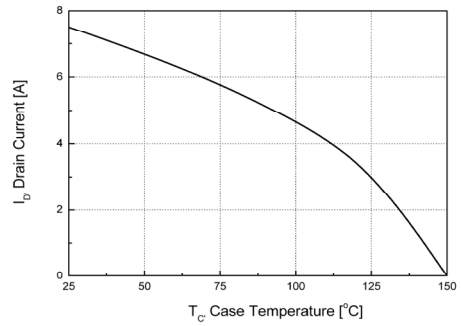


Fig 11-1 . Transient Thermal Response Curve fo TSP8N60M

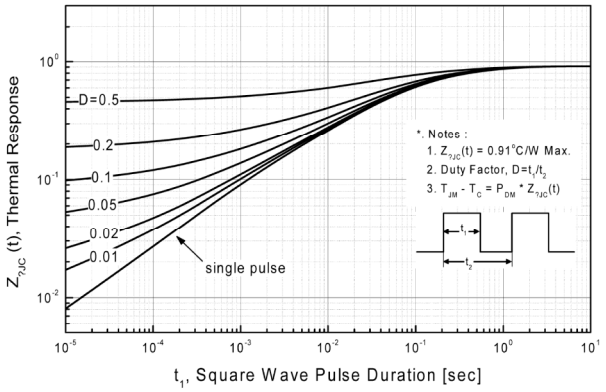


Fig 11-2 . Transient Thermal Response Curve for TSF8N60M

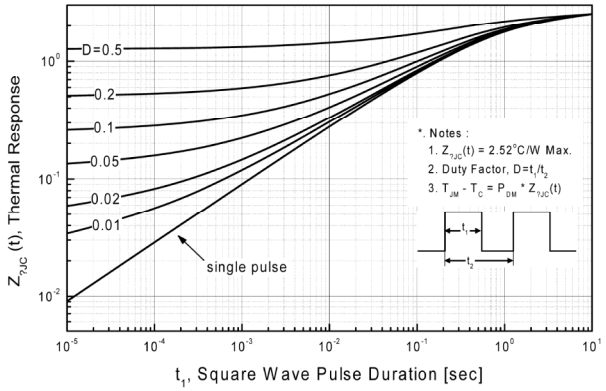


Fig. 12. Gate Charge Test Circuit & Waveforms

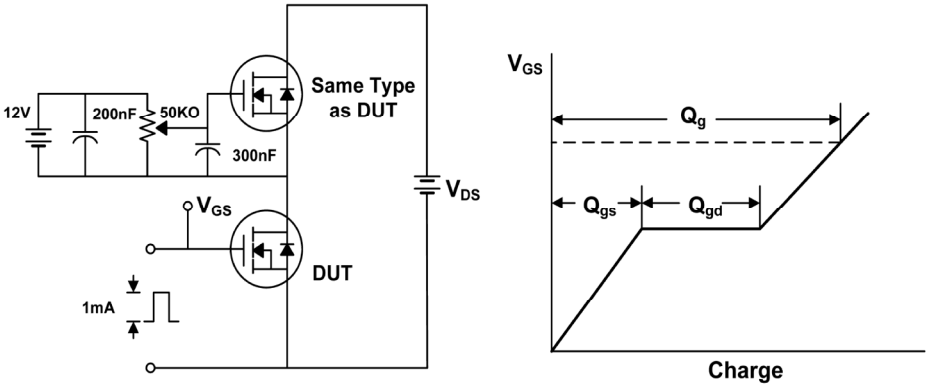


Fig 13. Switching Time Test Circuit & Waveforms

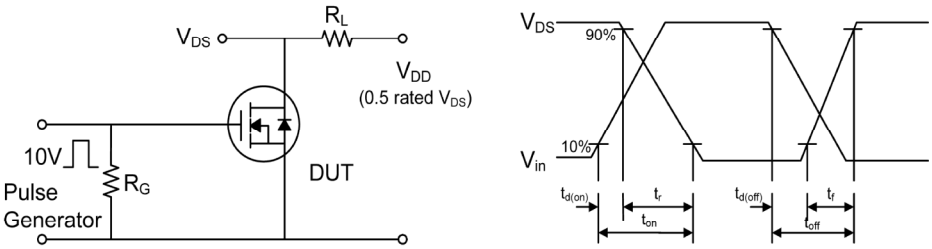


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

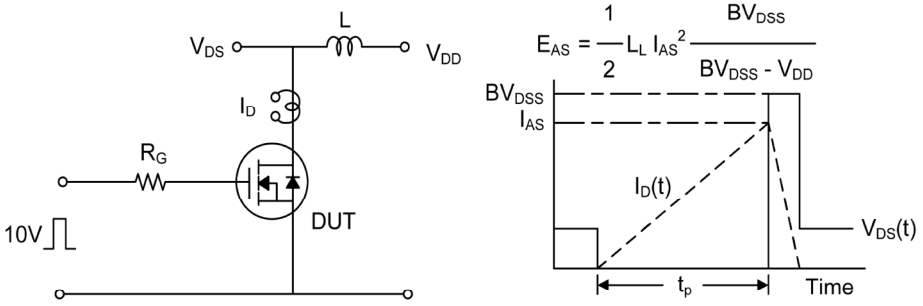


Fig. 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms