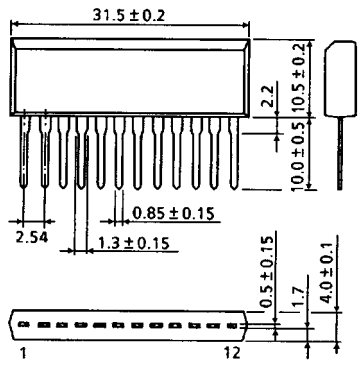
TOSHIBA Power MOS FET Module Silicon N Channel MOS Type (L^2-πMOSV 4 in 1)

MP4411

Industrial Applications

High Power, High Speed Switching Applications
For Printer Head Pin Driver and Pulse Motor Driver
For Solenoid Driver

Unit: mm



MOS FET		DIODE	
1, 5, 8, 12	GATE	2, 4, 9, 11	ANODE
2, 4, 9, 11	DRAIN	3, 10	CATHODE
6, 7	SOURCE		

JEDEC	—
JEITA	—
TOSHIBA	2-32C1D

Weight: 3.9 g (typ.)

- 4 V gate drive available
- Small package by full molding (SIP 12 pin)
- High drain power dissipation (4 devices operation)
  : P_T = 28 W (T_c = 25°C)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 0.28 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 3.5 S (typ.)
- Low leakage current: I_{GSS} = ±10 μA (max) (V_{GS} = ±16 V)
  I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement-mode: V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC	I_D	3	A
	Pulse	I_{DP}	12	
Drain power dissipation (1 device operation, Ta = 25°C)		P_D	2.2	W
Drain power dissipation (4 devices operation)	Ta = 25°C	P_{DT}	4.4	W
	Tc = 25°C		28	
Single pulse avalanche energy (Note 1)		E_{AS}	140	mJ
Avalanche current		I_{AR}	3	A
Repetitive avalanche energy (Note 2)	1 device operation	E_{AR}	0.22	mJ
	4 devices operation	E_{ART}	0.44	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

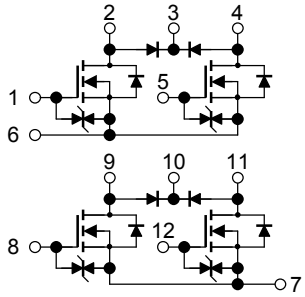
Note 1: Avalanche energy (single pulse) applied condition

V_{DD} = 50 V, starting T_{ch} = 25°C, L = 20 mH, R_G = 25 Ω, I_{AR} = 3 A

Note 2: Repetitive rating; pulse width limited by maximum channel temperature.

This transistor is an electrostatic sensitive device. Please handle with caution.

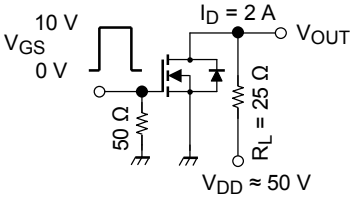
Array Configuration



Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance of channel to ambient (4 devices operation, Ta = 25°C)	$\Sigma R_{th\ (ch\text{-}a)}$	28.4	°C/W
Thermal resistance of channel to case (4 devices operation, Tc = 25°C)	$\Sigma R_{th\ (ch\text{-}c)}$	4.46	°C/W
Maximum lead temperature for soldering purposes (3.2 mm from case for t = 10 s)	T_L	260	°C

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 2 A	—	0.36	0.45	Ω
			V_{GS} = 10 V, I_D = 2 A	—	0.28	0.35	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 2 A	1.5	3.5	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	280	—	pF
Reverse transfer capacitance		C_{rss}		—	50	—	pF
Output capacitance		C_{oss}		—	105	—	pF
Switching time	Rise time	t_r		—	20	—	ns
	Turn-on time	t_{on}		—	50	—	
	Fall time	t_f		—	40	—	
	Turn-off time	t_{off}	V_{IN}: t_r, t_f < 5 ns, duty ≤ 1%, t_w = 10 μs	—	170	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 3 A	—	13.5	—	nC
Gate-source charge		Q_{gs}		—	8.5	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	5	—	nC

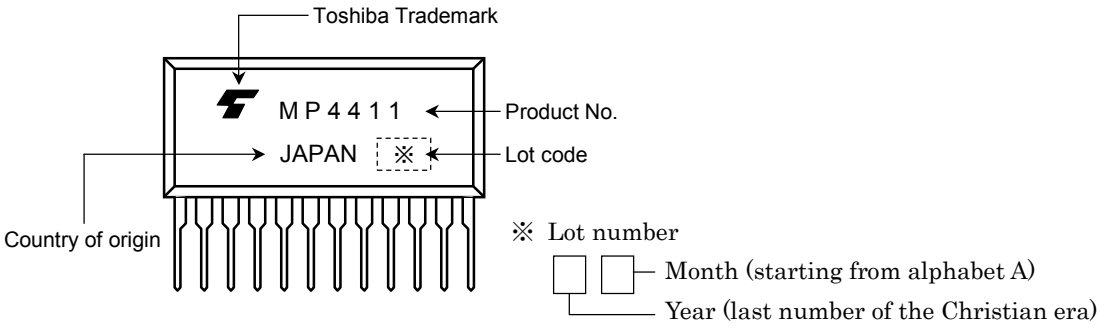
Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current	I_{DR}	—	—	—	3	A
Pulse drain reverse current	I_{DRP}	—	—	—	12	A
Diode forward voltage	V_{DSF}	IDR = 3 A, VGS = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	IDR = 3 A, VGS = 0 V, dIDR/dt = 50 A/μs	—	100	—	ns
Reverse recovery charge	Q_{rr}		—	0.2	—	μC

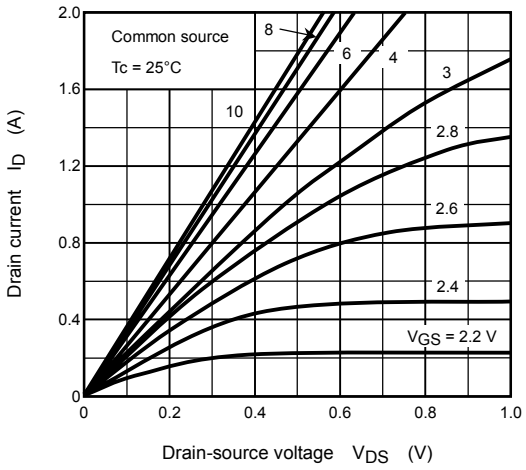
Flyback-Diode Rating and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward current	I_{FM}	—	—	—	3	A
Reverse current	I_R	VR = 100 V	—	—	0.4	μA
Reverse voltage	V_R	I_R = 100 μA	100	—	—	V
Forward voltage	V_F	I_F = 0.5 A	—	—	1.8	V

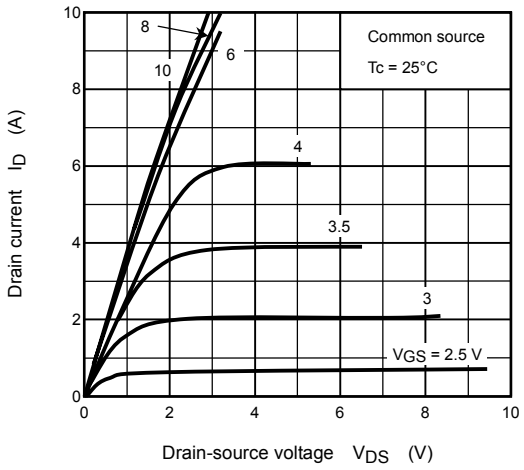
Marking



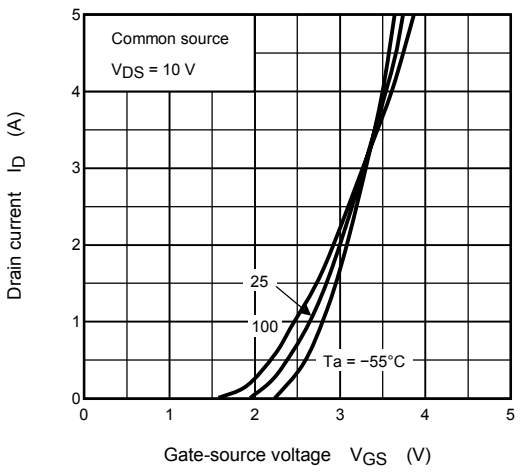
$I_D - V_{DS}$



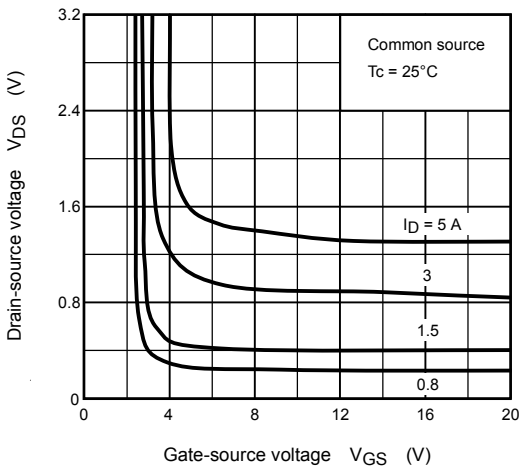
$I_D - V_{DS}$



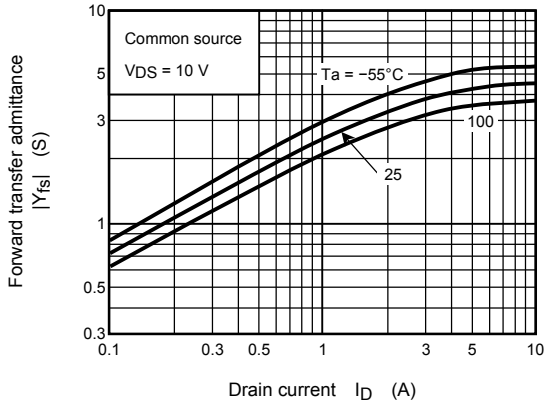
$I_D - V_{GS}$



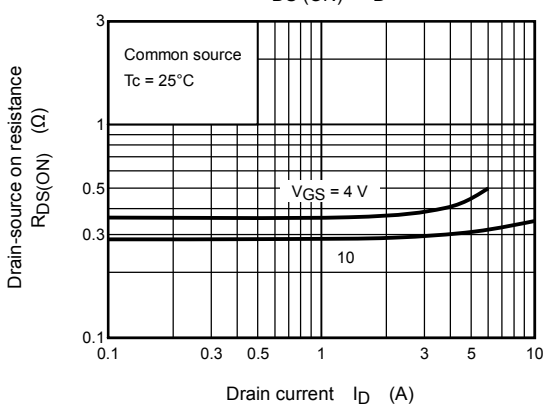
$V_{DS} - V_{GS}$



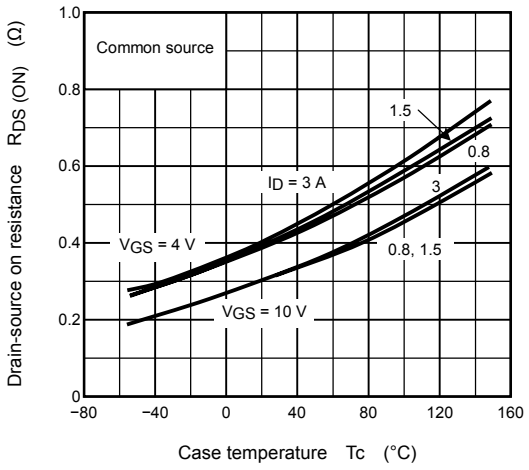
$|Y_{fs}| - I_D$



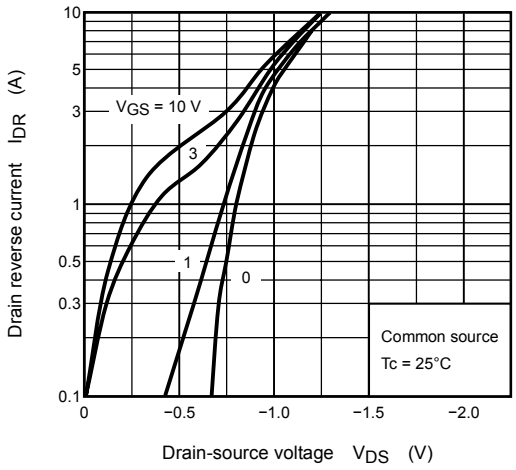
$R_{DS\ (ON)} - I_D$



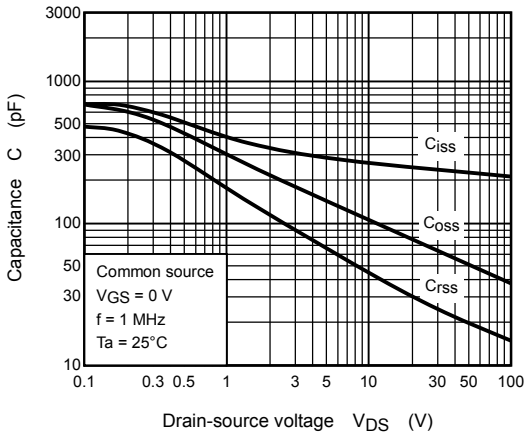
$R_{DS\ (ON)}$ – Tc



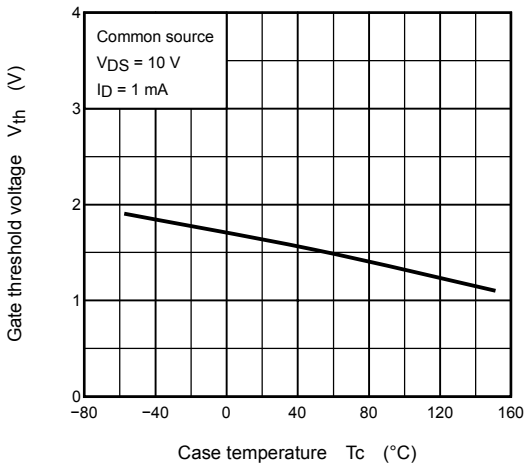
I_{DR} – V_{DS}



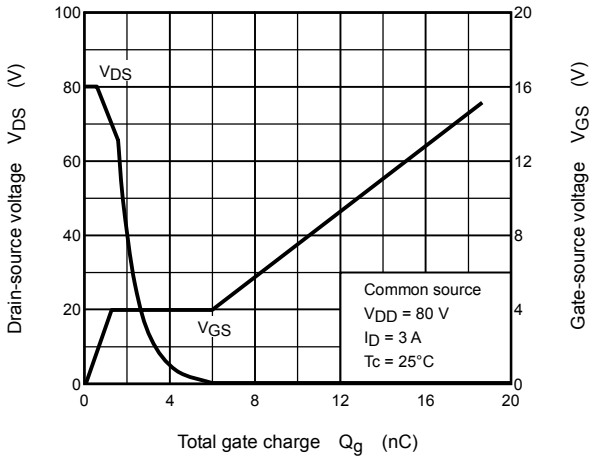
Capacitance – V_{DS}



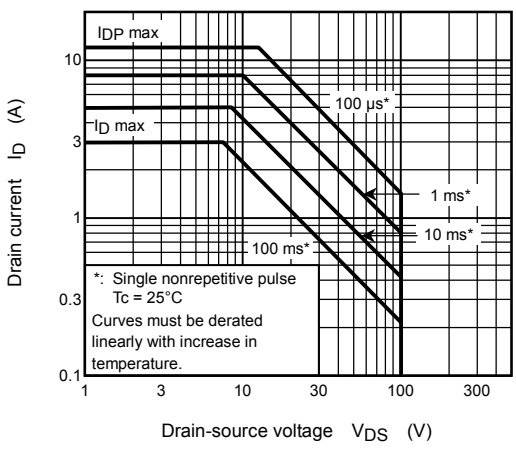
V_{th} – Tc



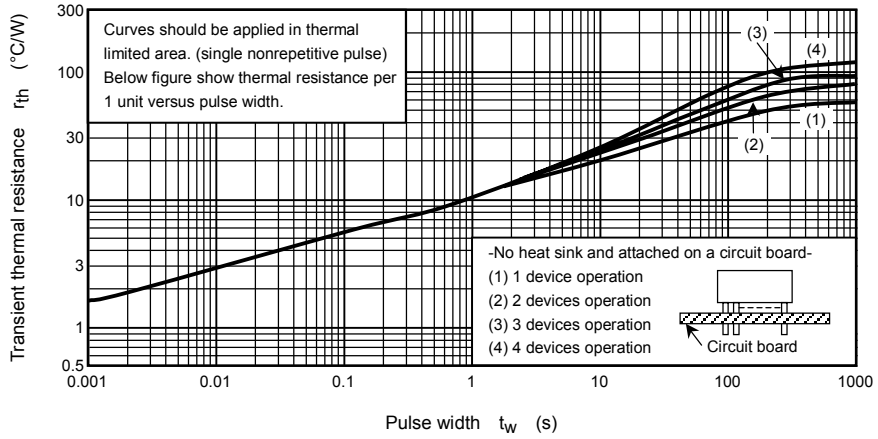
Dynamic Input/Output Characteristics



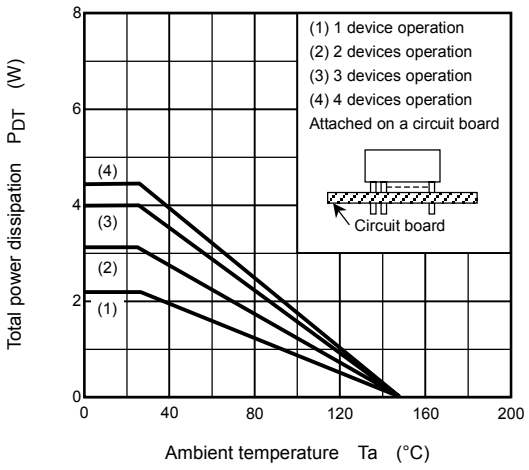
Safe Operating Area



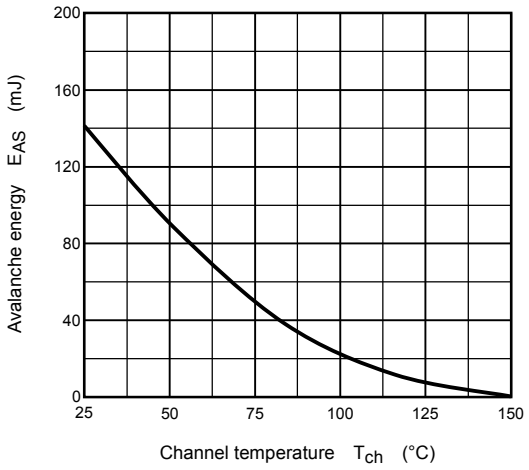
$r_{th} - t_w$



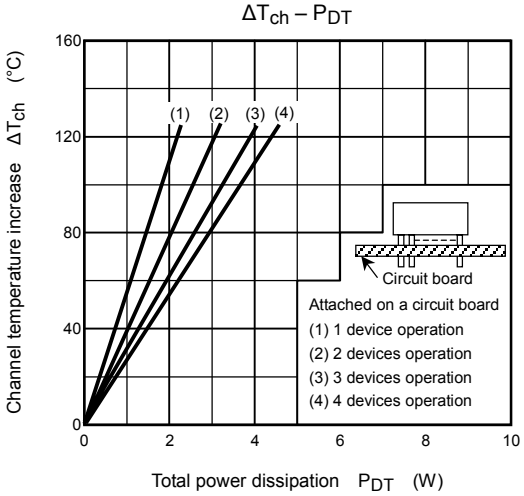
$P_{DT} - Ta$

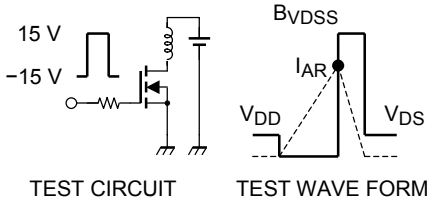


$E_{AS} - T_{cH}$



$\Delta T_{ch} - P_{DT}$





TEST CIRCUIT TEST WAVE FORM

Peak I_{AR} = 3 A, R_G = 25 Ω
V_{DD} = 50 V, L = 20 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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