1.5MHz, 1A Synchronous Step-Down Regulator

Halogen Free

General Description

The FP6161 is a high efficiency current mode synchronous buck PWM DC-DC regulator. The internal generated 0.6V precision feedback reference voltage is designed for low output voltage. Low $R_{DS(ON)}$ synchronous switch dramatically reduces conduction loss. To extend battery life for portable application, 100% duty cycle is supported for low-dropout operation. Shutdown mode also helps saving the current consumption. The FP6161 is packaged in DFN-6L, SOT23-5L, and TSOT23-5L to reduce PCB space.

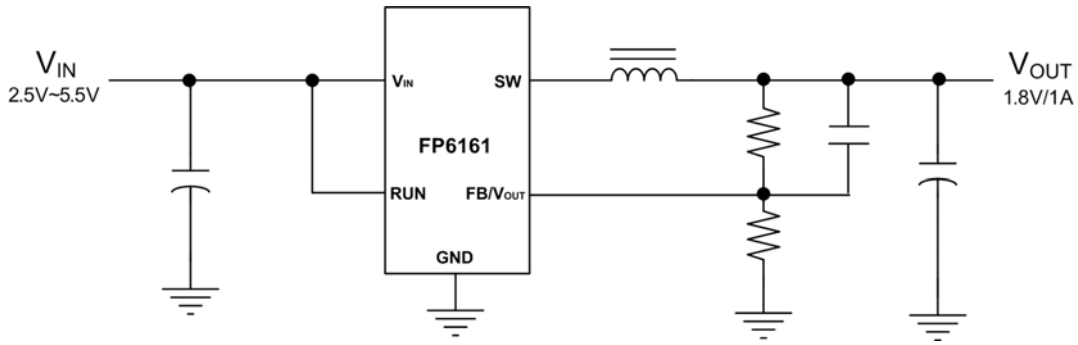
Features

- Input Voltage Range: 2.5 to 5.5V
- Precision Feedback Reference Voltage: 0.6V (±2%)
- Output Current: 1A(Max.)
- Duty Cycle: 0~100%
- Internal Fixed PWM Frequency: 1.5MHz
- Low Quiescent Current: 100μA
- No Schottky Diode Required
- Built-in Soft Start
- Current Mode Operation
- Over temperature Protection
- Package: DFN-6L(2x2mm), SOT23-5L, TSOT23-5L

Applications

- Cellular Telephone
- Wireless and DSL Modems
- Digital Still Cameras
- Portable Products
- MP3 Players

Typical Application Circuit



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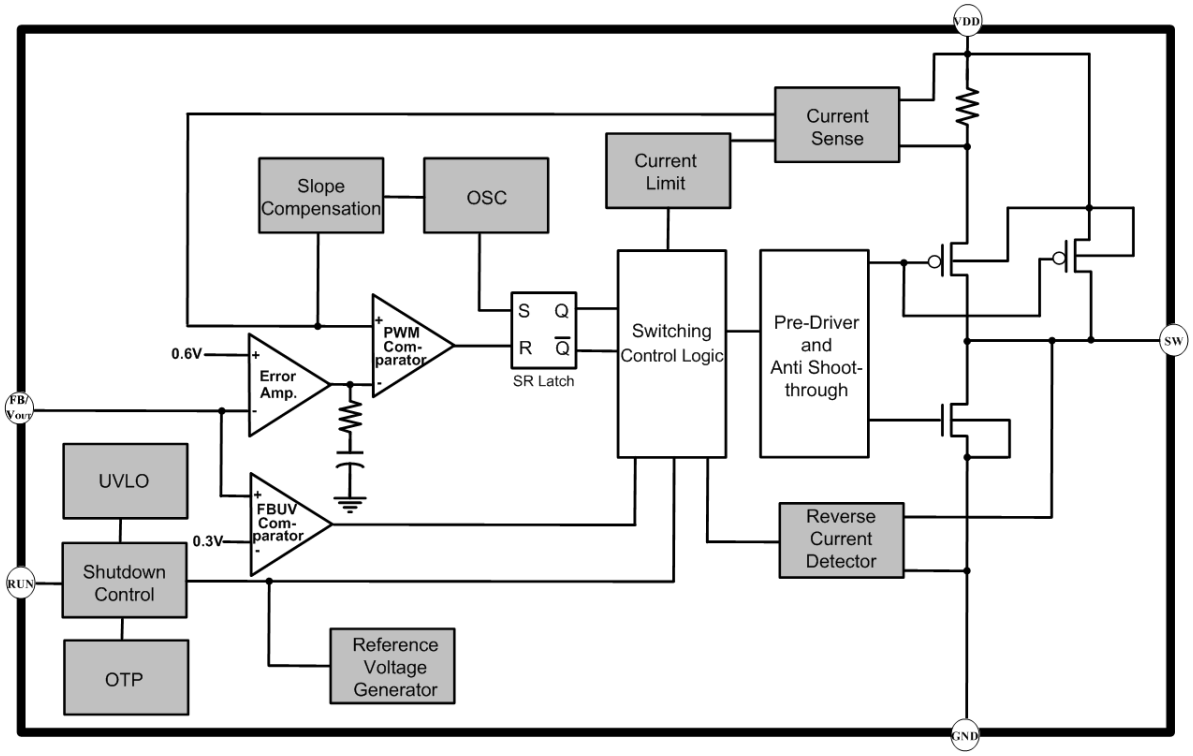
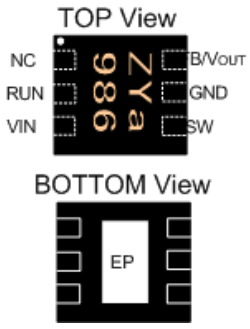
Function Block Diagram



Marking View

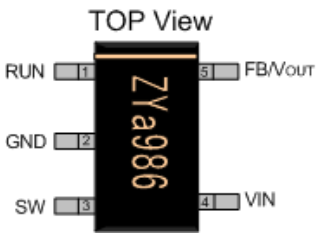
DFN-6L



Pin Descriptions

Name	No.	I/O	Description
NC	1	-	No Connect
RUN	2	I	Enable Pin
VIN	3	P	Power Supply
SW	4	O	Switch
GND	5	P	Ground
FB/VOUT	6	I	Feedback Pin
EP	7	P	Exposed PAD – must connect to Ground

SOT23-5L/TSOT23-5L



Name	No.	I/O	Description
RUN	1	I	Enable Pin
GND	2	P	Ground
SW	3	O	Switch
VIN	4	P	Power Supply
FB/VOUT	5	I	Feedback Pin

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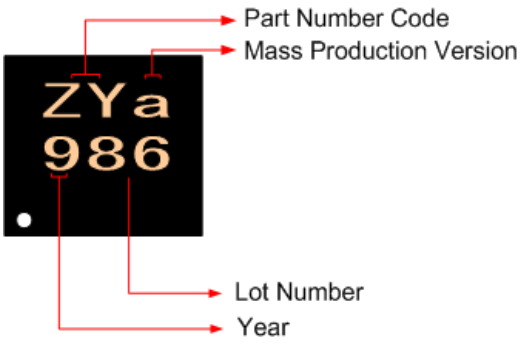
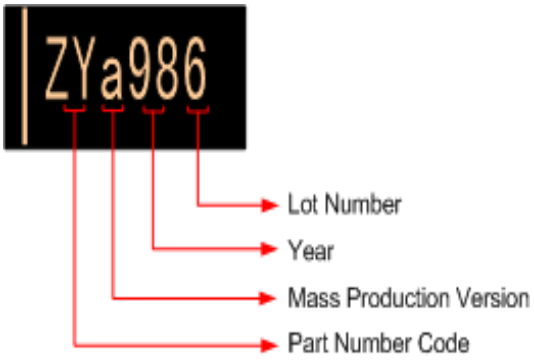
IC Date Code Distinguish

DFN-6L



SOT23-5L/TSOT23-5L



NOTE:

Lot Number
(It is the last two numbers of wafer lot number.)
Example:
132371TB →71

Per-Half Month
Example:
January → A(Front Half Month),B(Last Half Month)
February → C(Front Half Month),D(Last Half Month)

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Order Information

Part Number	Code	Operating Temperature	Package	Description
FP6161d-LF-ADJ	ZY	-40°C ~ +85°C	DFN-6L(2x2mm)	Bag
FP6161dR-LF-ADJ	ZY			Tape & Reel
FP6161d-LF-1.5V	ZW	-40°C ~ +85°C	DFN-6L(2x2mm)	Bag
FP6161dR-LF-1.5V	ZW			Tape & Reel
FP6161d-LF-1.8V	ZX	-40°C ~ +85°C	DFN-6L(2x2mm)	Bag
FP6161dR-LF-1.8V	ZX			Tape & Reel
FP6161K-LF-ADJ	ZY	-40°C ~ +85°C	SOT23-5L	Bag
FP6161KR-LF-ADJ	ZY			Tape & Reel
FP6161K-LF-1.5V	ZW	-40°C ~ +85°C	SOT23-5L	Bag
FP6161KR-LF-1.5V	ZW			Tape & Reel
FP6161K-LF-1.8 V	ZX	-40°C ~ +85°C	SOT23-5L	Bag
FP6161KR-LF-1.8 V	ZX			Tape & Reel
FP6161a-LF-ADJ	ZY	-40°C ~ +85°C	TSOT23-5L	Bag
FP6161aR-LF-ADJ	ZY			Tape & Reel
FP6161a-LF-1.5V	ZW	-40°C ~ +85°C	TSOT23-5L	Bag
FP6161aR-LF-1.5V	ZW			Tape & Reel
FP6161a-LF-1. 8V	ZX	-40°C ~ +85°C	TSOT23-5L	Bag
FP6161aR-LF-1.8V	ZX			Tape & Reel

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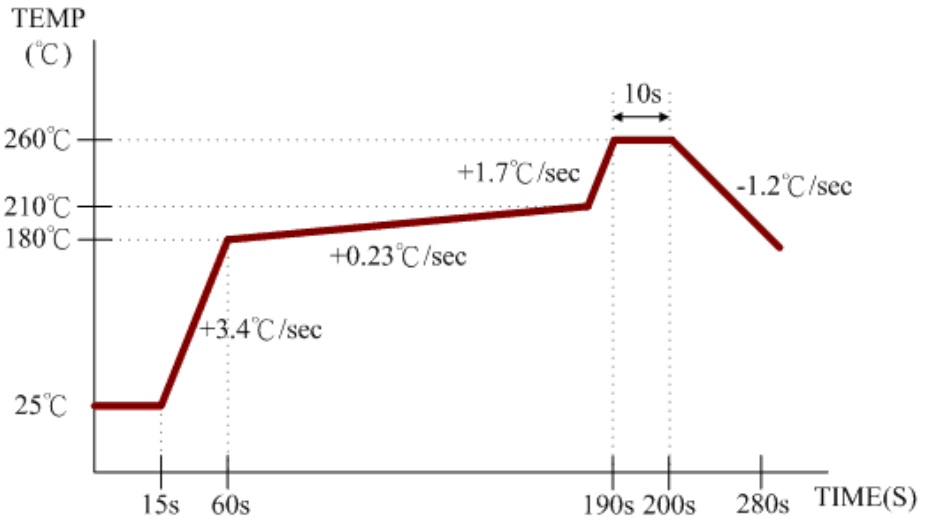
Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Supply Voltage	V_{IN}	-	-0.3		6	V
RUN, VFB, SW Voltage		-	-0.3		V_{IN}	V
P-Channel Switch Source Current (DC)					1	A
N-Channel Switch Source Current (DC)					1	A
Peak SW Switch Sink and Source Current (AC)					2	A
Thermal Resistance (Junction to Ambient)	θ_{JA}	DFN-6L			+165	°C/W
		SOT23-5L			+250	°C/W
		TSOT23-5L			+250	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	DFN-6L			+20	°C/W
		SOT23-5L			+90	°C/W
		TSOT23-5L			+90	°C/W
Operating temperature			–40		+85	°C
Junction Temperature					+150	°C
Storage temperature			–65		+150	°C
Lead Temperature (soldering, 10 sec)		DFN-6L			+260	°C
		SOT23-5L			+260	°C
		TSOT23-5L			+260	°C

IR Re-flow Soldering Curve



IR Re-flow Soldering Curve

NOTE:

1. Suggest IR Reflow Soldering Profile Condition.

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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{IN}	-	2.5	-	5.5	V
Operating Temperature		-	-40	-	85	°C

DC Electrical Characteristics (T_A= 25°C, V_{IN}=3.6V, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Regulated Feedback Voltage	V_{FB}	T_A=25°C	0.588	0.6	0.612	V
		-40°C~+85°C	0.585	0.6	0.615	V
Line Regulation with VREF	ΔV_{FB}	V_{IN}=2.5V to 5.5V		0.04	0.4	%/V
Regulated Output Voltage	V_{OUT}	FP6161-1.5, I_{OUT}=100mA	1.455	1.5	1.545	V
		FP6161-1.8, I_{OUT}=100mA	1.746	1.8	1.845	V
Output Voltage LineRegulation	ΔV_{OUT}	V_{IN}=2.5 to 5.5V		0.04	0.4	%/V
RDS(ON) of P-Channel FET	$R_{DS(ON)}P$	I_{SW}=100mA		0.28	0.35	Ω
RDS(ON) of N-Channel FET	$R_{DS(ON)}N$	I_{SW} =-100mA		0.25	0.32	Ω
SW Leakage	I_{LSW}	V_{RUN}=0V, V_{IN}=5V		±0.01	±1	μA
Peak Inductor Current	I_{PK}	V_{FB}=0.5V	1.125	1.5	1.875	A
Input Voltage Range	V_{IN}	-40°C~+85°C	2.5		5.5	V
Quiescent Current	I_{CC}	Shutdown, V_{RUN}=0V		0.1	1	μA
		Active, V_{FB}=0.5V, V_{RUN}=V_{IN}		100		μA
		PFM, V_{FB}=0.7V, V_{RUN}=V_{IN}		80		μA
RUN Threshold	V_{RUN}	-40°C ~+85°C	0.3	1	1.5	V
RUN Leakage Current	I_{RUN}	-40°C ~+85°C		±0.01	±1	μA
Oscillator Frequency	F_{OSC}	V_{FB}=0.6V, -40°C~+85°C	1.2	1.5	1.8	MHz

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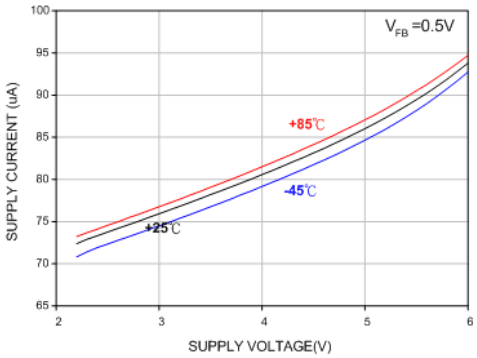
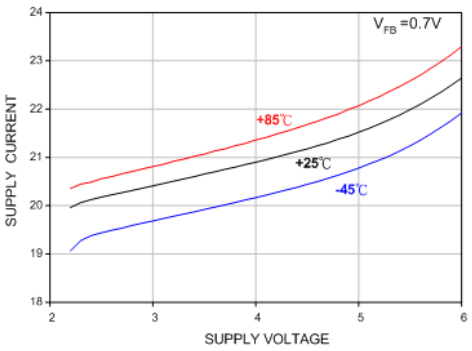
Typical Operating Characteristics

(T_A= 25°C, V_{IN}=3.6V, unless otherwise noted)

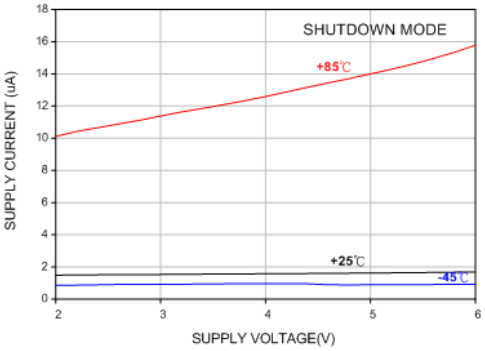
SUPPLY CURRENT vs SUPPLY VOLTAGE



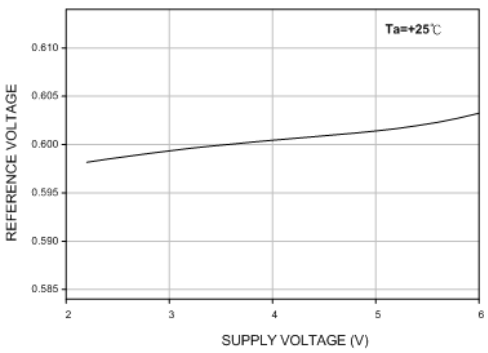
SUPPLY CURRENT vs SUPPLY VOLTAGE



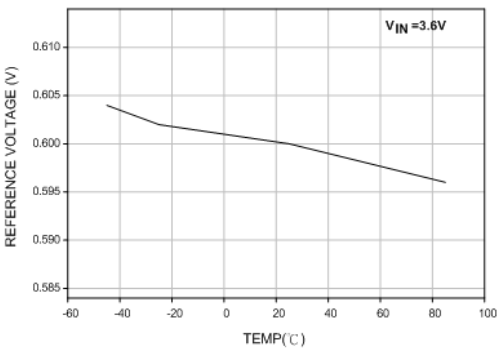
SUPPLY CURRENT vs SUPPLY VOLTAGE



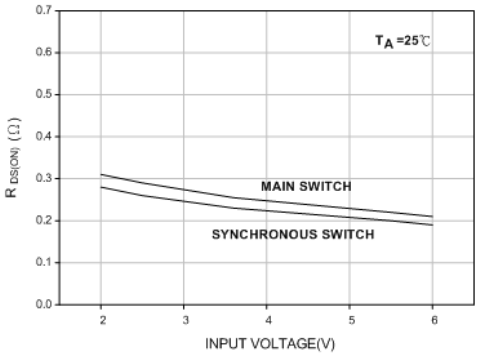
REFERENCE VOLTAGE vs SUPPLY VOLTAGE



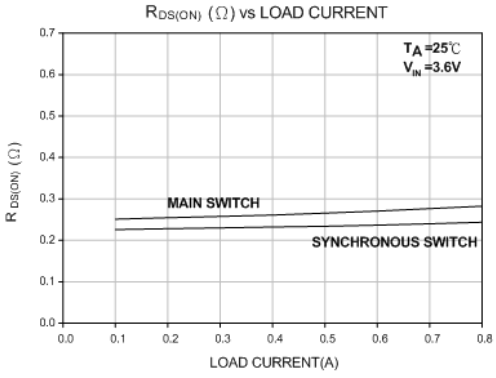
REFERENCE VOLTAGE vs TEMPERATURE



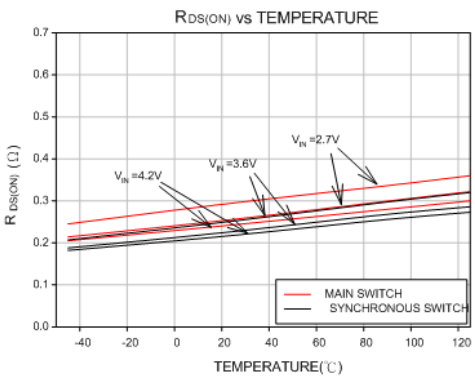
R_DS(ON) (Ω) vs INPUT VOLTAGE(V)



R_DS(ON) (Ω) vs LOAD CURRENT



R_DS(ON) vs TEMPERATURE



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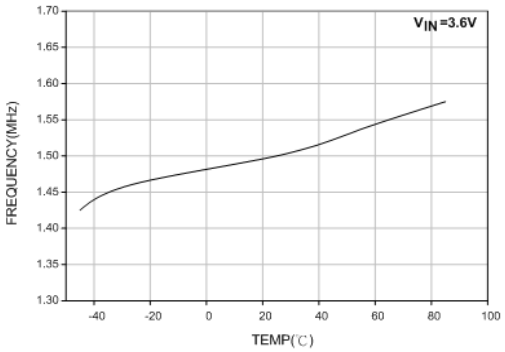
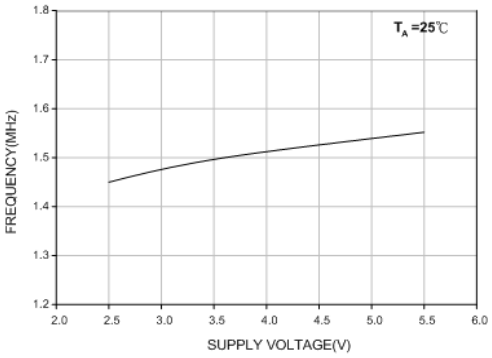
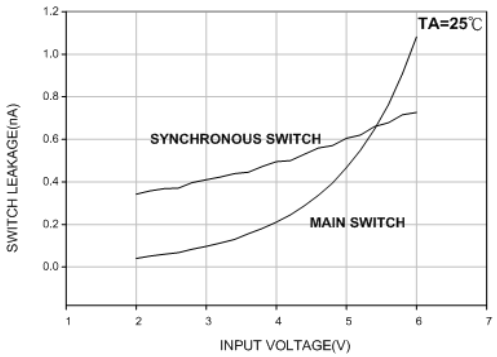
OSCILLATOR FREQUENCY vs TEMPERATURE



FREQUENCY vs SUPPLY VOLTAGE



SWITCH LEAKAGE vs INPUT VOLTAGE



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Function Description

Control Loop

The FP6161 is a high efficiency current mode synchronous buck regulator. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are built internally. With current mode operation, the PWM duty is controlled both by the error amplifier output and the peak inductor current. At the beginning of each cycle, the oscillator turn on the P-MOSFET switch to source current from V_{IN} to SW output. Then, the chip starts to compare the inductor current with the error amplifier output. Once the inductor current is larger than the error amplifier output, the P-MOSFET switch is turned off. When the load current increases, the feedback voltage FB will slightly drop. This causes the error amplifier to output a higher current level until the prior mentioned peak inductor current reach the same level. The output voltage then can be sustained at the same.

When the top P-MOSFET switch is off, the bottom synchronous N-MOSFET switch is turned on. Once the inductor current reverses, both top and bottom MOSFET will be turn off to leave the SW pin into high impedance state.

The FP6161's current mode control loop also contains slope compensation to suppress sub-harmonic oscillations at high duty cycles. This slope compensation is achieved by adding a compensation ramp to the inductor current signal.

LDO Mode

The FP6161's maximum duty cycle can reach 100%. That means the driver main switch is turn on through out whole clock cycle. Once the duty reaches 100%, the feedback path no longer controls the output voltage. The output voltage will be the input voltage minus the main switch voltage drop.

Over Current Protection

FP6161 limits the peak main switch current cycle by cycle. When over current happens, chip will turn off the main switch and turn the synchronous switch on until next cycle.

Short Circuit Protection

When the FB pin is drop below 300mV, the chip will tri-state the output pin SW automatically. After 300us rest to avoid over heating, chip will re-initiate PWM operation with soft start.

Thermal Protection

FP6161 will shutdown automatically when the internal junction temperature reaches 150℃ to protect both the part and the system.

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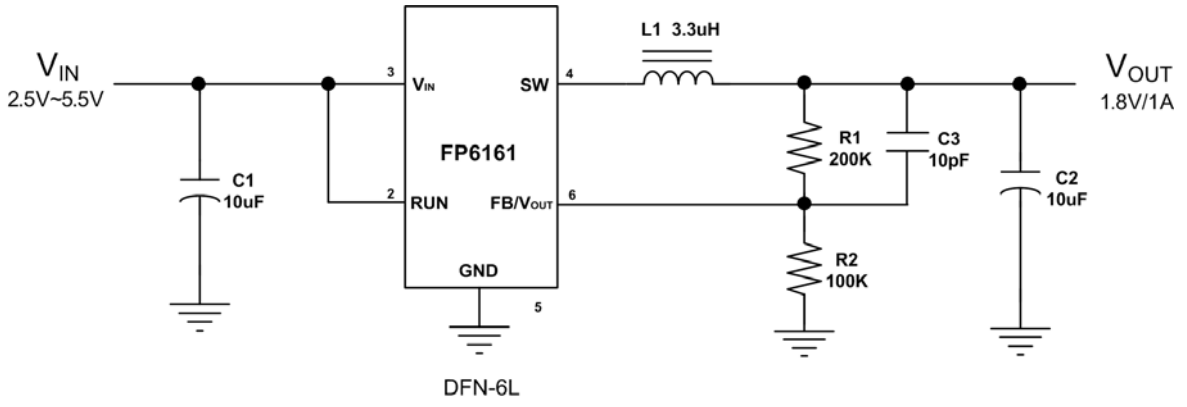
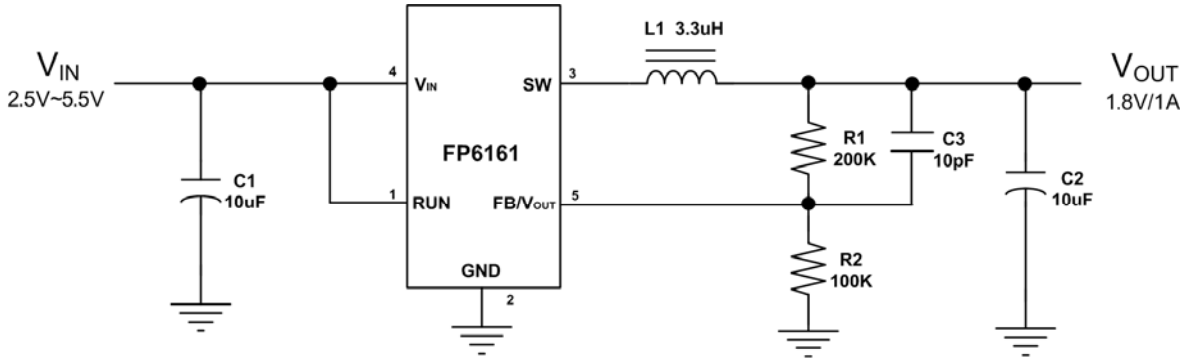
Application Information



DFN-6L



SOT23-5L/TSOT23-5L

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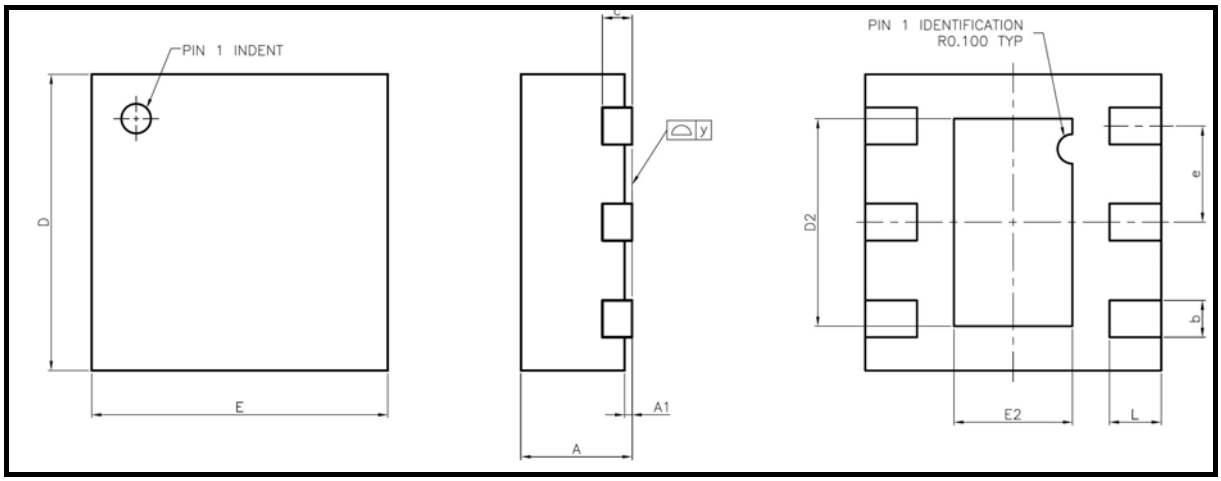
Package Outline

DFN-6L



Symbols	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.19	0.20	0.25
D	1.95	2.00	2.05
D2	1.35	1.40	1.45
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
e	-	0.65	-
L	0.30	0.35	0.40
y	0.00	-	0.075

UNIT: mm

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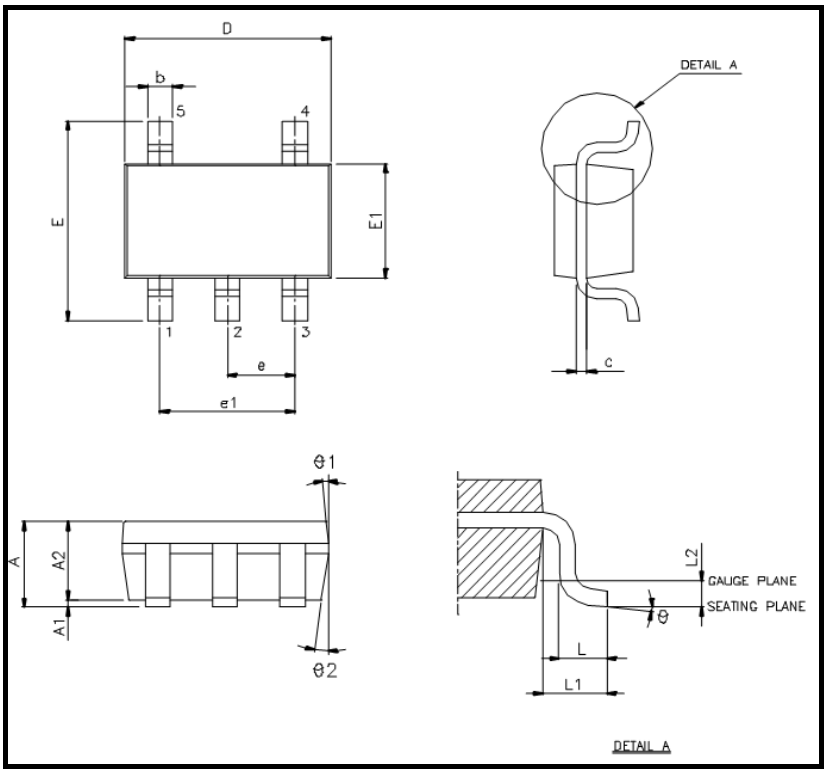
SOT23-5L



Symbols	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.25	0.50
c	0.08	0.20
D	2.70	3.00
E	2.60	3.00
E1	1.05	1.70
e	0.95 BSC.	
e1	1.90 BSC.	
L	0.30	0.55
L1	0.60 REF.	
L2	0.25 BSC.	
θ°	0	10

UNIT: mm

NOTE:

1.JEDEC OUTLINE:MO-178 AA.

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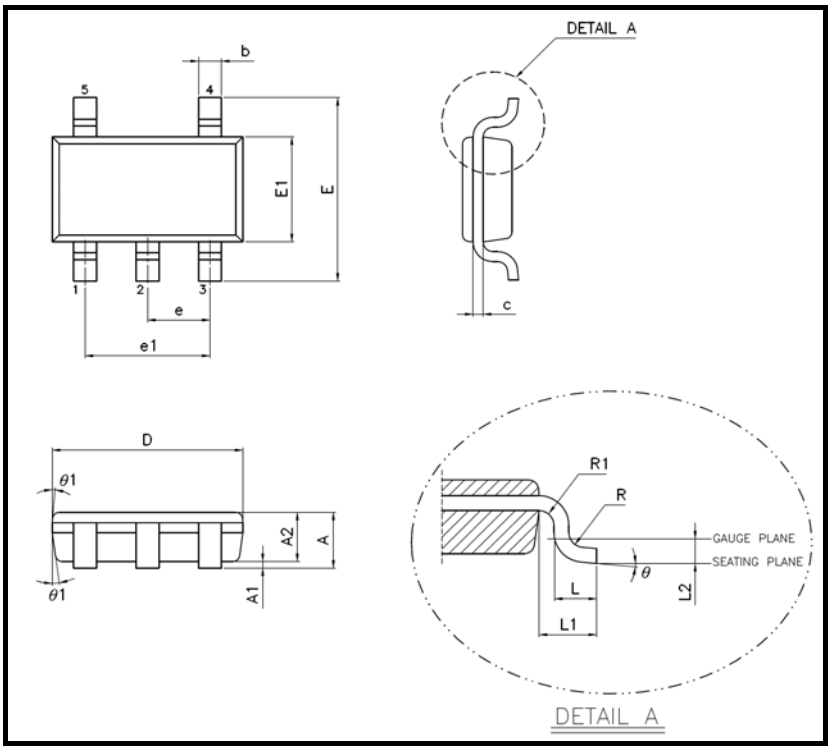
TSOT23-5L



Symbols	Min.	Max.
A	0.75	0.80
A1	0.00	0.50
A2	0.70	0.775
b	0.35	0.50
c	0.10	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.05	1.70
e	0.95 BSC.	
e1	1.90 BSC.	
L	0.37	0.60
L1	0.60 REF.	
L2	0.25 BSC.	
R	0.10	-
R1	0.10	0.25
θ	0	8
Θ1	4	12

NOTE:

UNIT: mm

1.JEDEC OUTLINE:MO-193 AA

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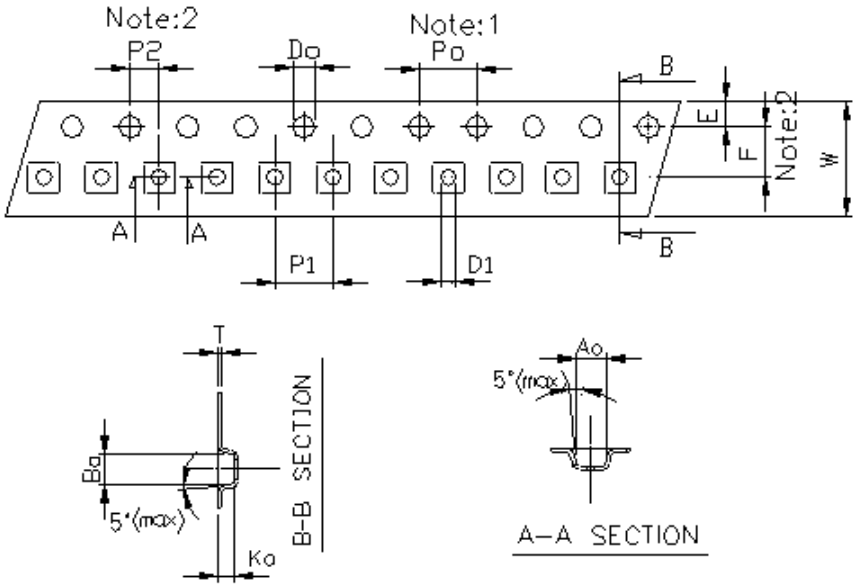
Carrier Tape Dimensions

DFN-6L



Symbols	Min.	Max.
K1	-	-
P_O	4.00	0.10
P1	4.00	0.10
P2	2.00	0.05
D_O	1.05	0.10
D1	1.10	0.10
E	1.75	0.10
F	3.50	0.05
$10P_O$	40.0	0.10
W	8.00	0.20
T	0.25	0.02

UNIT: mm

NOTE:

1. 10 Sprocket holes pitch cumulative tolerance is ±0.1mm.
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a place 0.3mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1mm per 100mm through a length of 250mm.

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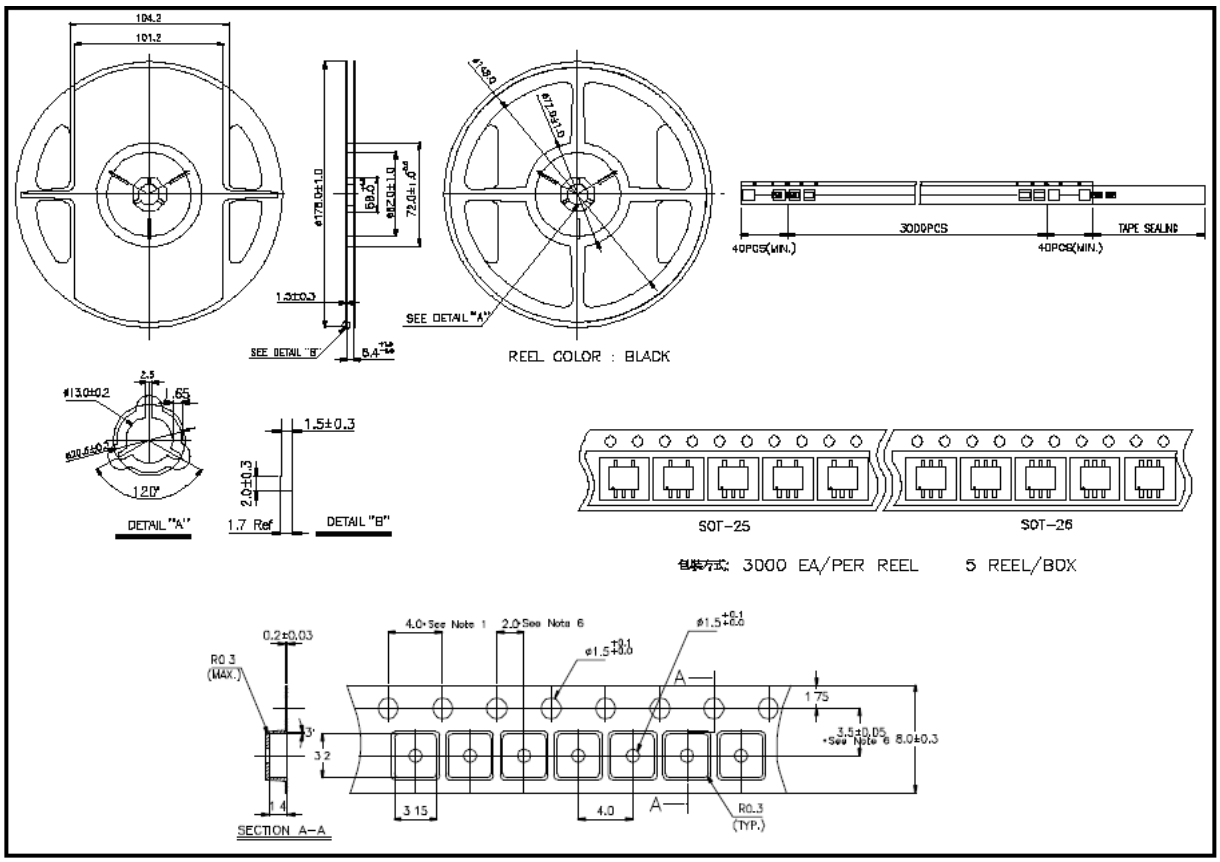
SOT23-5L



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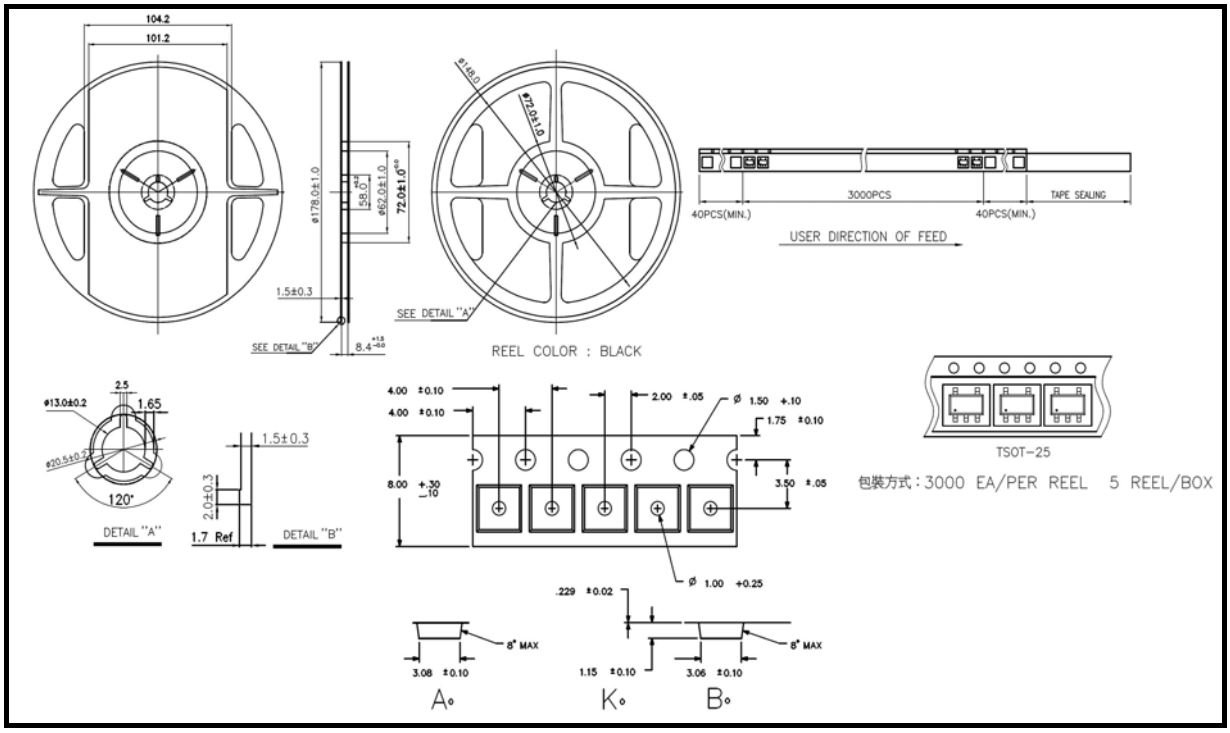
TSOT23-5L



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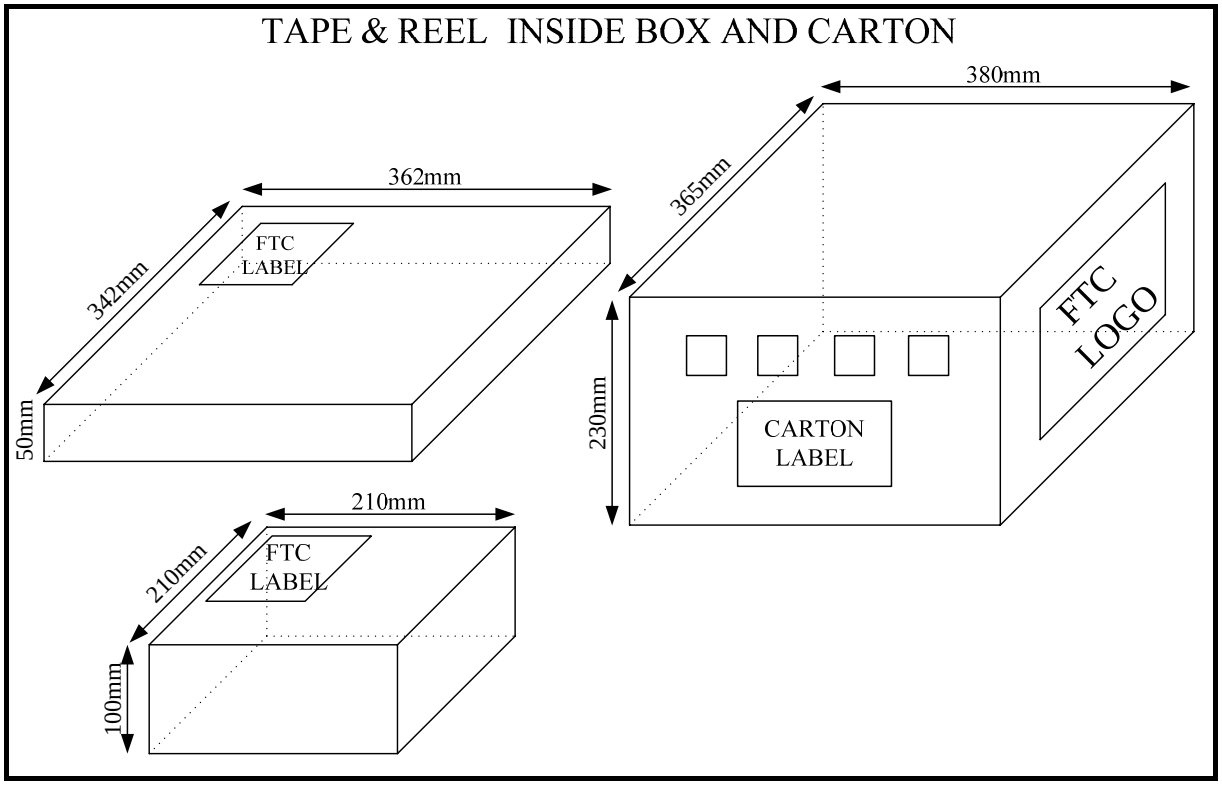
Packing Specifications

Box Dimension



Tape & Reel Inside Box and Carton

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Packing Quantity Specifications

DFN-6L

FP6161dR-LF-ADJ	FP6161dR-LF-1.5V	FP6161dR-LF-1.8V
2500 EA/Reel	2500 EA/Reel	2500 EA/Reel
4 Reels / Inside Box	4 Reels / Inside Box	4 Reels / Inside Box
4 Inside Boxes / Carton	4 Inside Boxes / Carton	4 Inside Boxes / Carton

SOT23-5L

FP6161KR-LF-ADJ	FP6161KR-LF-1.5V	FP6161KR-LF-1.8V
2500 EA/Reel	2500 EA/Reel	2500 EA/Reel
4 Reels / Inside Box	4 Reels / Inside Box	4 Reels / Inside Box
4 Inside Boxes / Carton	4 Inside Boxes / Carton	4 Inside Boxes / Carton

TSOT23-5L

FP6161aR-LF-ADJ	FP6161aR-LF-1.5V	FP6161aR-LF-1.8V
2500 EA / Reel	2500 EA / Reel	2500 EA / Reel
4 Reels / Inside Box	4 Reels / Inside Box	4 Reels / Inside Box
4 Inside Boxes / Carton	4 Inside Boxes / Carton	4 Inside Boxes / Carton

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