

P-Channel Enhancement Mode Field Effect Transistor

● Features

$V_{DS}(V) = -30V$, $I_D = -4.2A$,

$R_{DS(ON)} = 52m\Omega$ @ $V_{GS} = -10V$.

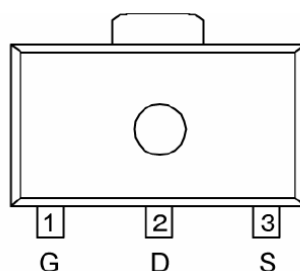
$R_{DS(ON)} = 68m\Omega$ @ $V_{GS} = -4.5V$.

High density cell design for low $R_{DS(ON)}$.

● General Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

● Pin Configurations



SOT-89
(TOP VIEW)

● Absolute Maximum Ratings @ $T_A = 25^\circ C$ unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	± 20	V
Drain Current (Note 1)	Continuous $T_A = 25^\circ C$	I_D	-4.2	A
	Pulsed (Note 2)		-50	A
Total Power Dissipation (Note 1)		P_D	1000	mW
Operating and Storage Junction Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ C$

● **Electrical Characteristics** @T_A=25°C unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μ A	-30	-34		V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V		-3	-200	nA
Gate–Body Leakage Current	I _{GSS}	V _{GS} = ± 20 V, V _{DS} = 0 V		±1.5	±50	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = -250 μ A	-1	-1.3	-3	V
Drain–Source On–State Resistance	R _{DS(ON)}	V _{GS} = -10 V, I _D = -5 A		52	65	mΩ
		V _{GS} = -4.5 V, I _D = -4 A		68	85	
Forward Transconductance	G _{FS}	V _{DS} = -5 V, I _D = -6 A		12		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} = -15 V, V _{GS} = 0 V, F = 1.0 MHz		550		pF
Output Capacitance	C _{OSS}		--	60		
Reverse Transfer Capacitance	C _{RSS}			50		
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	T _{D(ON)}	V _{DS} = -15 V, R _L = 2.5 Ω, V _{GS} = -10V, R _{GEN} =3 Ω		8.6		nS
Turn–Off Delay Tim	T _{D(OFF)}			28.2		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1 A		-0.81		V

Notes

- 1、Pulse width limited by maximum junction temperature.
- 2、Pulse test: PW ≤ 300 μs, duty cycle ≤ 2%.
- 3、Guaranteed by design, not subject to production testing.
- 4、Surface Mounted on FR4 Board, T < 5 sec.

● **Typical Performance Characteristics** (T_J = 25°C Noted)

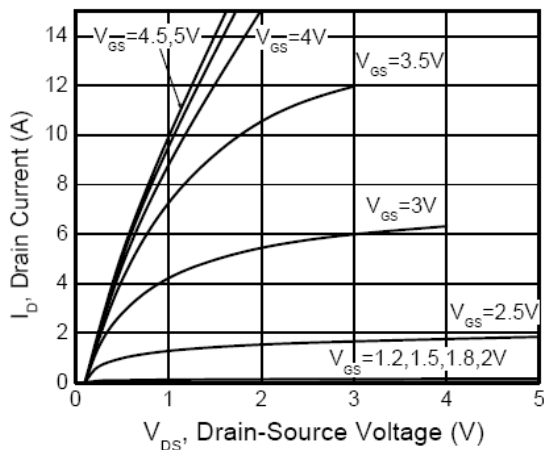


Figure 1. Output Characteristics

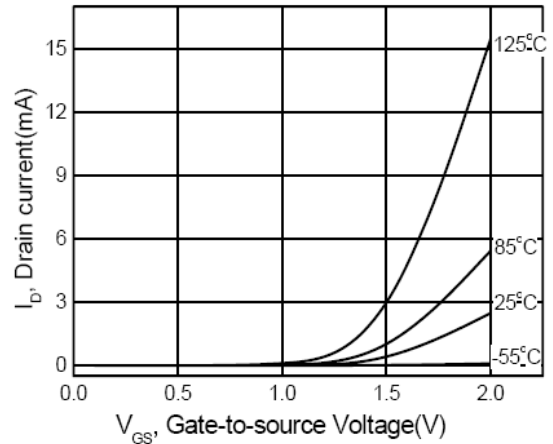


Figure 2. Transfer Characteristics

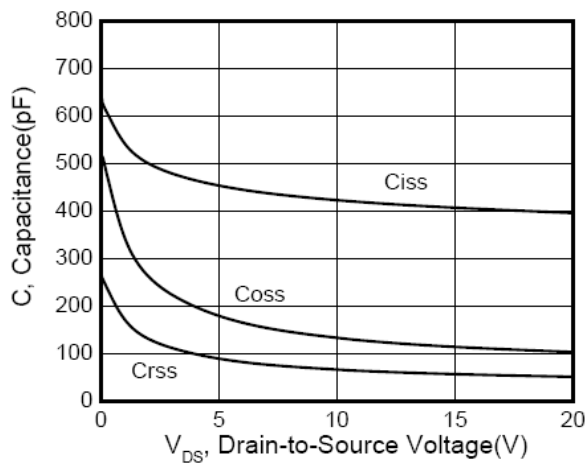


Figure 3. Capacitance

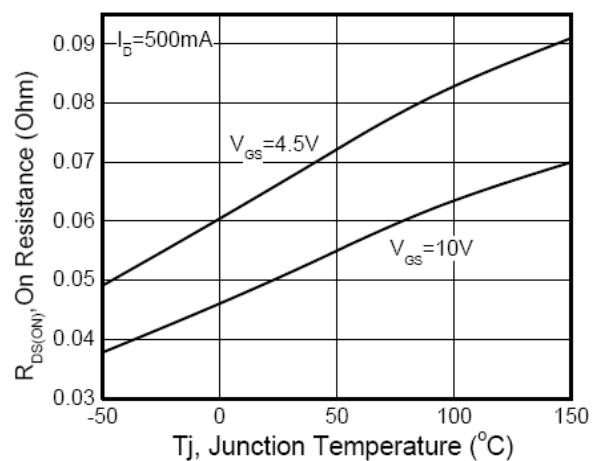


Figure 4. On Resistance Vs. Temperature

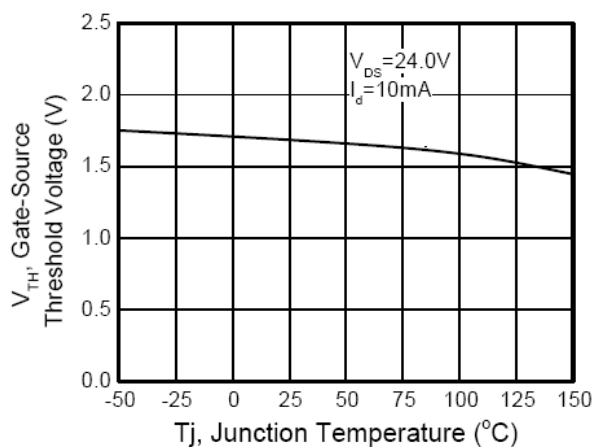


Figure 5. Gate Threshold Vs. Temperature

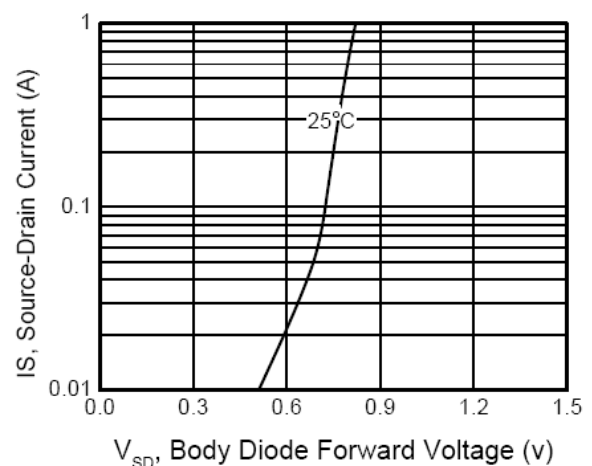
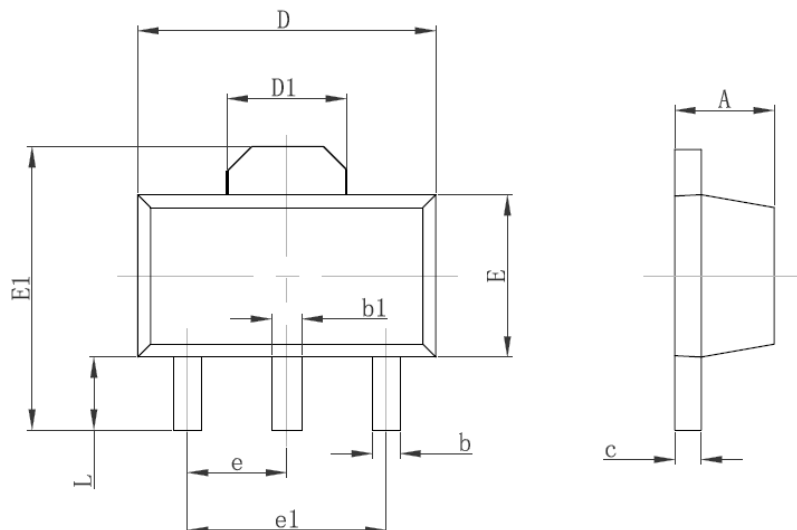


Figure 6. Body Diode Forward Voltage

- Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060TYP	
e1	3.000 TYP		0.118TYP	
L	0.900	1.200	0.035	0.047

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