32K x 8 LOW POWER CMOS STATIC RAM

MARCH 2004

FEATURES

- High-speed access time: 20 ns
- Low active power: 200 mW (typical)
- Low standby power:
  250 µW (typical) CMOS standby
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V power supply
- Temperature Offerings:
  Option A1: –40°C to +85°C
  Option A2: –40°C to +105°C
  Option A3: –40°C to +125°C

DESCRIPTION

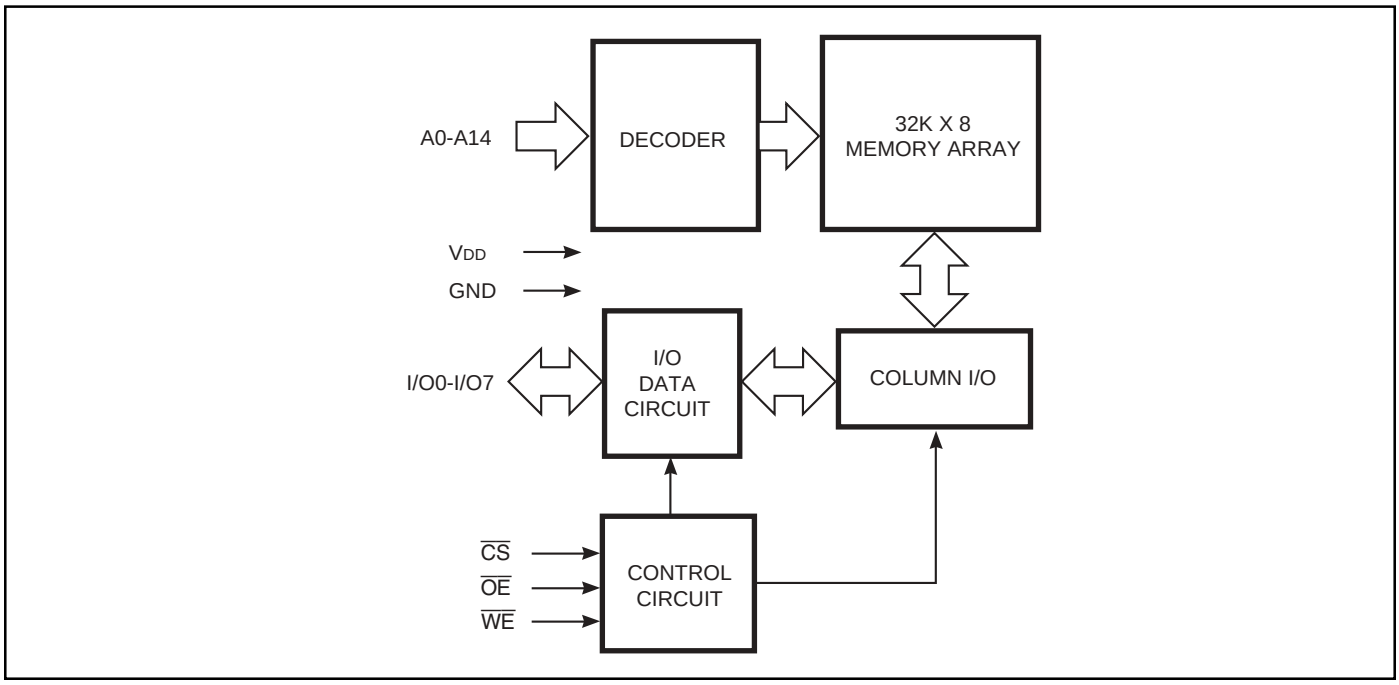
The *ISSI* IS65C256 is a low power, 32,768 word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance, low power CMOS technology.

When CS is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 µW (typical) at CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Select (CS) input and an active LOW Output Enable (OE) input. The active LOW Write Enable (WE) controls both writing and reading of the memory.

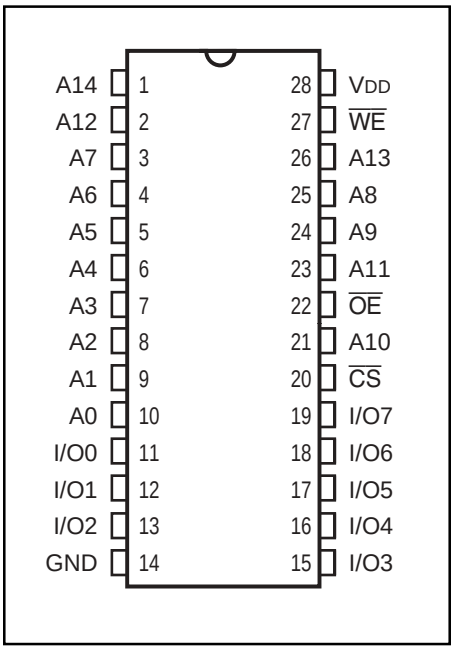
The IS65C256 is Packaged in the JEDEC Standard 28-Pin SOP and 28-Pin TSOP (Type I).

FUNCTIONAL BLOCK DIAGRAM



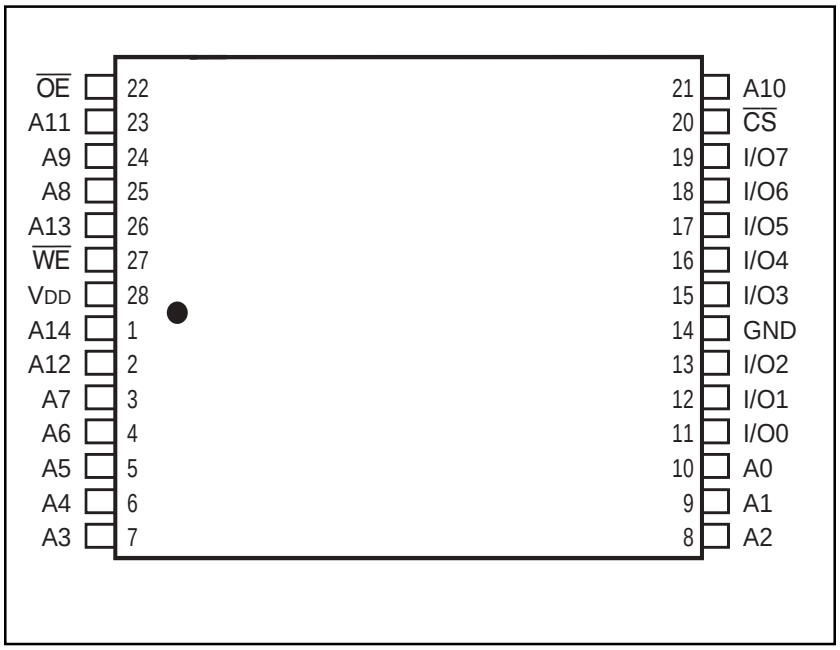
PIN CONFIGURATION

32-Pin SOP



PIN CONFIGURATION

32-Pin TSOP (Type 1)



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V_{DD}
A1	–40°C to +85°C	5V ± 10%
A2	–40°C to +105°C	5V ± 10%
A3	–40°C to +125°C	5V ± 10%

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –1.0 mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 2.1 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]		–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	–10	10	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	–10	10	µA

Note:
1. V_{IL} = –3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-20 ns Min.	-20 ns typ[2]	-20 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA, f = 0	A1	—		40	mA
			A2	—		50	
			A3	—		60	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA, f = f_{MAX}	A1	—	25	95	mA
			A2	—	25	105	
			A3	—	25	115	
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL}, $\overline{CS}$ = V_{IH}, f = 0	A1	—		5	mA
			A2	—		10	
			A3	—		10	
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS}$ ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	A1	—		0.5	mA
			A2	—		1.0	
			A3	—		1.5	

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 5V, T_A = 25°C, t_{AA} = 70 ns, and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 5.0V.

DATA RETENTION CHARACTERISTICS

Symbol	Parameter	Test Conditions	Options	Min.	typ [1]	Max.	Units
V_{DR}	V_{DD} for retention of data			2.0		—	V
I_{DR1}	Data retention current	V_{DR} = 3.0V	A1	—	50	150	µA
I_{DR2}	Data retention current	V_{DR} = 3.0V	A2	—	50	300	µA
I_{DR3}	Data retention current	V_{DR} = 3.0V	A3	—	50	500	µA

Note:
2. Typical values are measured at V_{DD} = 3V, T_A = 25°C, and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

		-20 ns		
Symbol	Parameter	Min.	Max.	Unit
t_{RC}	Read Cycle Time	20	—	ns
t_{AA}	Address Access Time	—	20	ns
t_{OHA}	Output Hold Time	3	—	ns
t_{ACS}	$\overline{CS}$ Access Time	—	20	ns
t_{DOE}	$\overline{OE}$ Access Time	—	8	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	0	9	ns
t_{LZCS}[2]	$\overline{CS}$ to Low-Z Output	3	—	ns
t_{HZCS}[2]	$\overline{CS}$ to High-Z Output	0	9	ns
t_{PU}[3]	$\overline{CS}$ to Power-Up	0	—	ns
t_{PD}[3]	$\overline{CS}$ to Power-Down	—	18	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

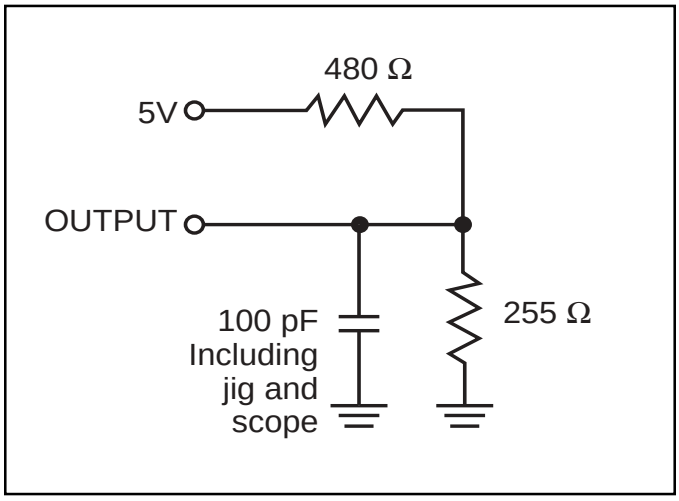


Figure 1.

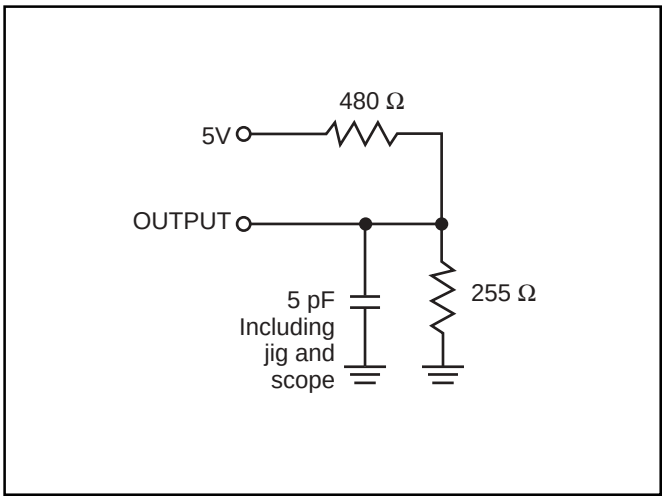
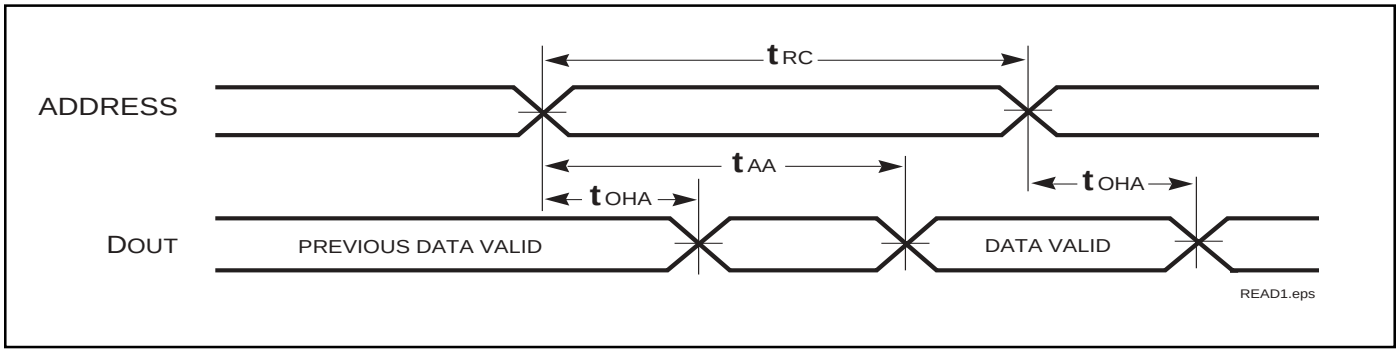


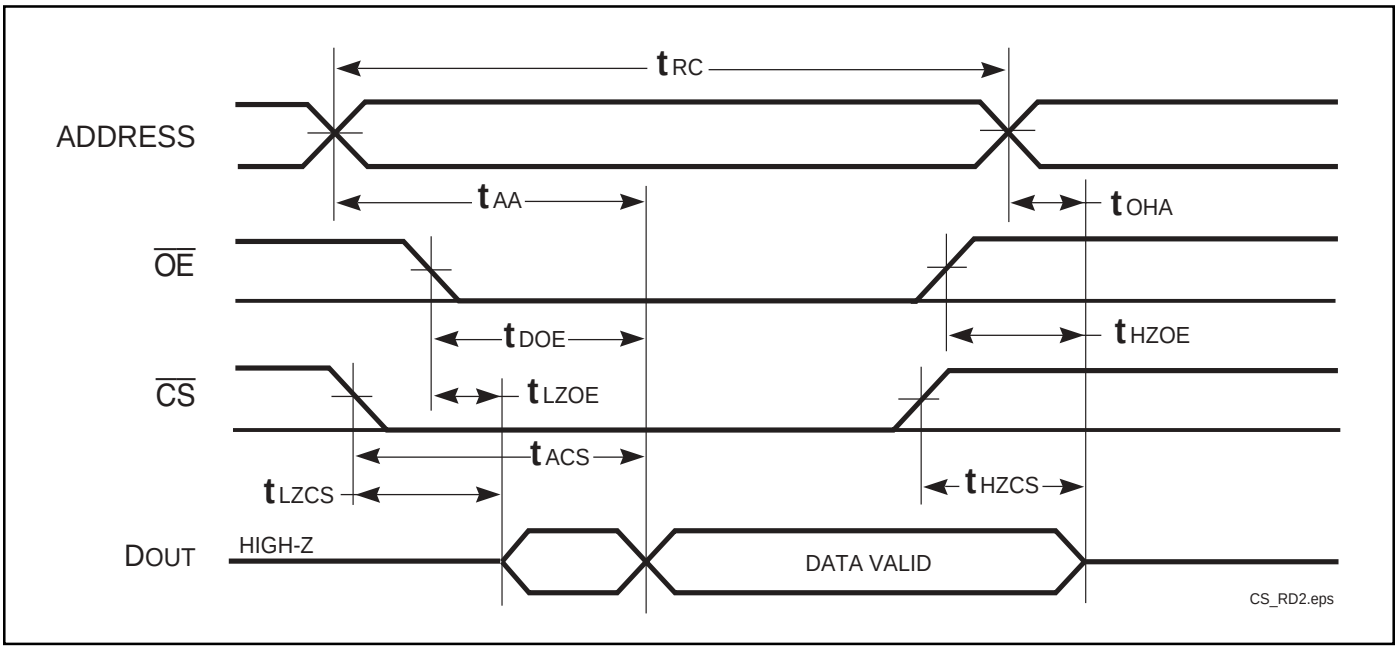
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CS}$ LOW transitions.

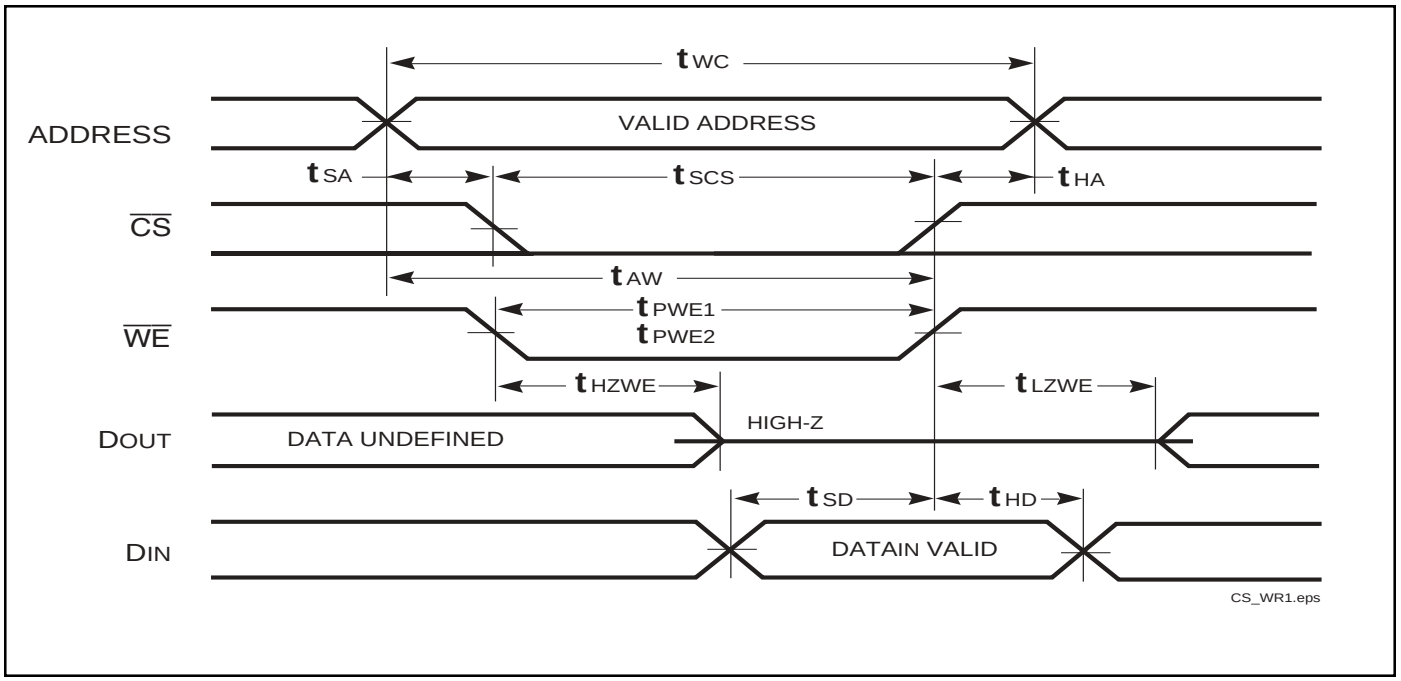
WRITE CYCLE SWITCHING CHARACTERISTICS[1,3] (Over Operating Range)

		-20 ns		
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
t_{WC}	Write Cycle Time	20	—	ns
t_{SCS}	$\overline{CS}$ to Write End	13	—	ns
t_{AW}	Address Setup Time to Write End	15	—	ns
t_{HA}	Address Hold from Write End	1	—	ns
t_{SA}	Address Setup Time	0	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	13	—	ns
t_{SD}	Data Setup to Write End	10	—	ns
t_{HD}	Data Hold from Write End	0	—	ns

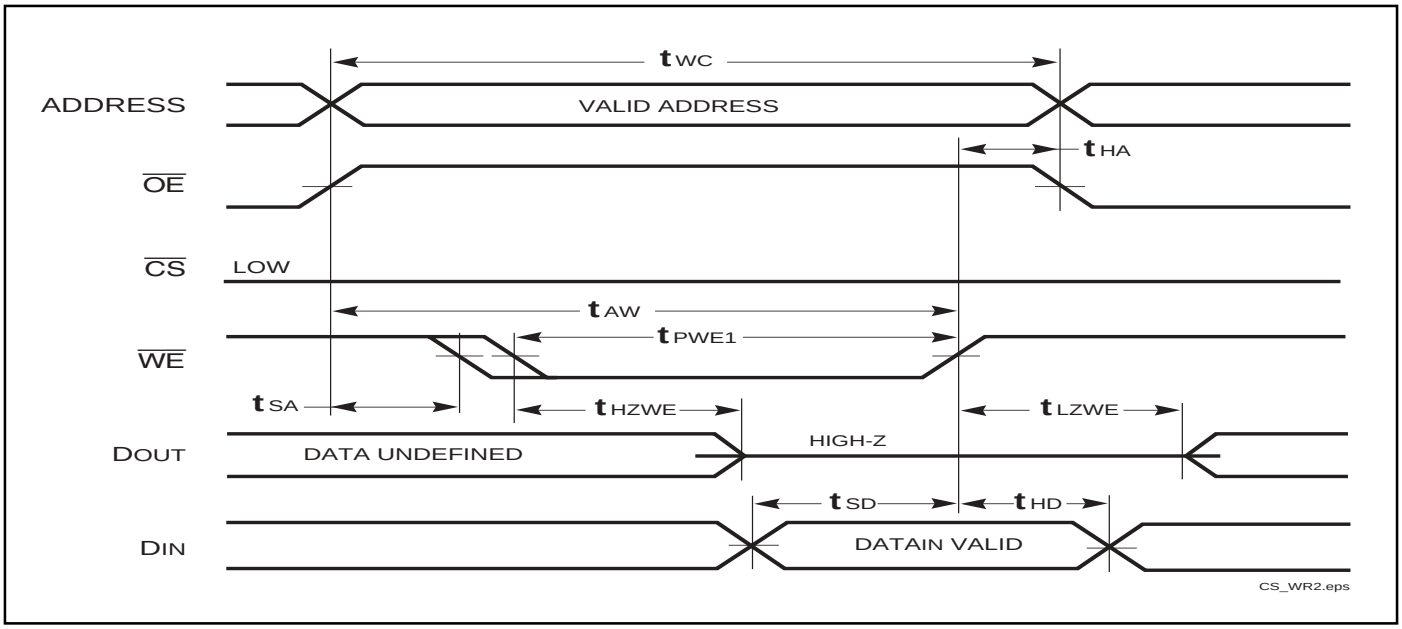
Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with $\overline{OE}$ HIGH.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{CS}$ Controlled, $\overline{OE}$ is HIGH or LOW) (1)



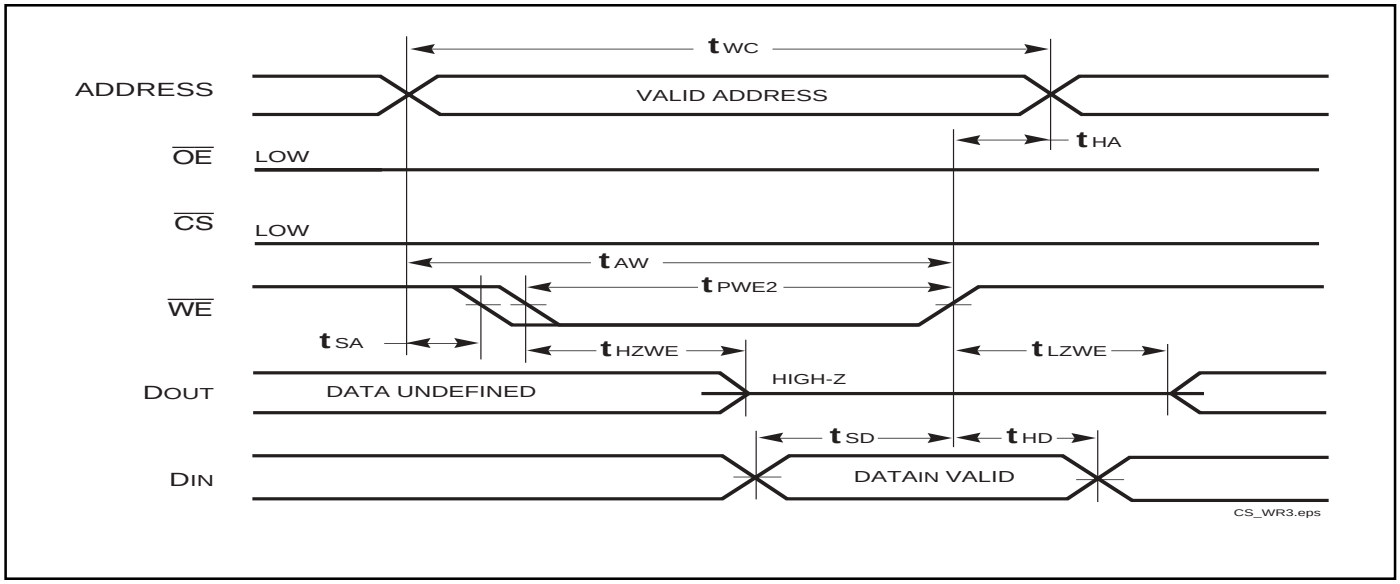
WRITE CYCLE NO. 2 ($\overline{OE}$ is HIGH During Write Cycle) (1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE}$ = V_{IH}.

ORDERING INFORMATION

Temperature Range (A1): –40°C to +85°C

Speed (ns)	Order Part No.	Package
20	IS65C256-20TA1	TSOP

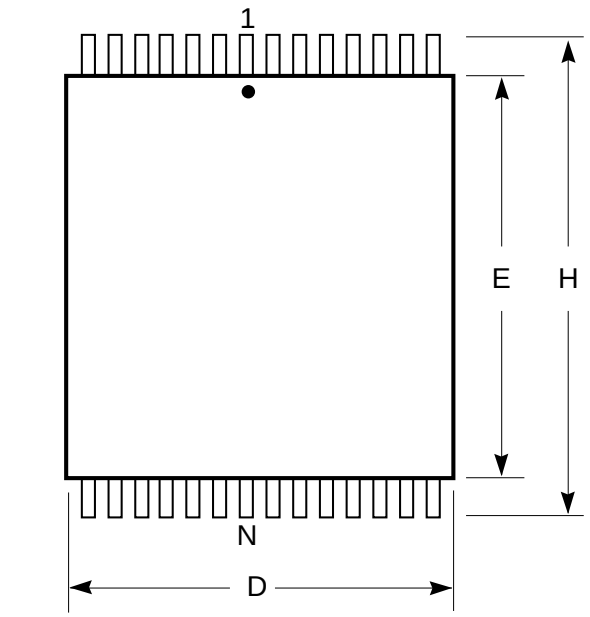
Temperature Range (A2): –40°C to +105°C

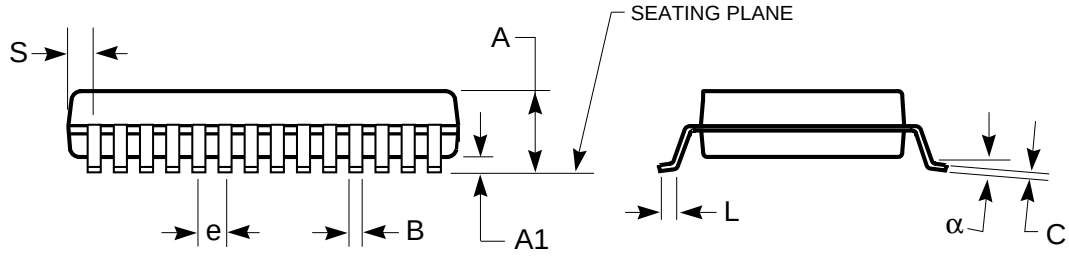
Speed (ns)	Order Part No.	Package
20	IS65C256-20TA2	TSOP
	IS65C256-20UA2	Plastic SOP

Temperature Range (A3): –40°C to +125°C

Speed (ns)	Order Part No.	Package
20	IS65C256-20TA3	TSOP
	IS65C256-20UA3	Plastic SOP

Plastic TSOP - 28-pins
Package Code: T (Type I)



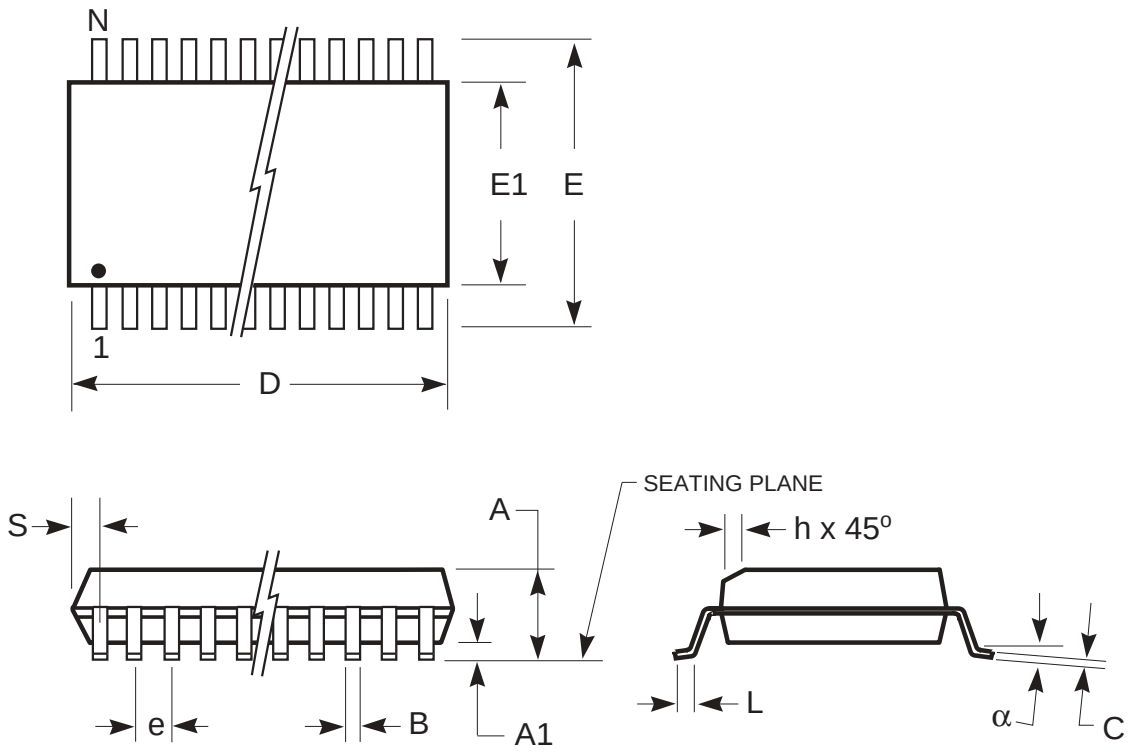


Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		28		
A	1.00	1.20	0.037	0.047
A1	0.05	0.20	0.002	0.008
B	0.16	0.27	0.006	0.011
C	0.10	0.20	0.004	0.008
D	7.90	8.10	0.308	0.316
E	11.70	11.90	0.456	0.465
H	13.20	13.60	0.515	0.531
e	0.55 BSC		0.022 BSC	
L	0.30	0.70	0.011	0.027
α	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PACKAGING INFORMATION

330-mil Plastic SOP
Package Code: U (28-pin)



	MILLIMETERS		INCHES	
Sym.	**Min.**	**Max.**	**Min.**	**Max.**
No. Leads	**28**		**28**	
A	—	2.84	—	0.112
A1	0.10	—	0.004	—
B	0.36	0.51	0.014	0.020
C	0.25	—	0.010	—
D	17.98	18.24	0.708	0.718
E	11.51	12.12	0.453	0.477
E1	8.28	8.53	0.326	0.336
e	1.27 BSC		0.050 BSC	
h	0.30	0.51	0.012	0.020
L	0.71	1.14	0.028	0.045
α	0°	8°	0°	8°
S	0.58	1.19	0.023	0.047

Notes:
1. Controlling dimension: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.