

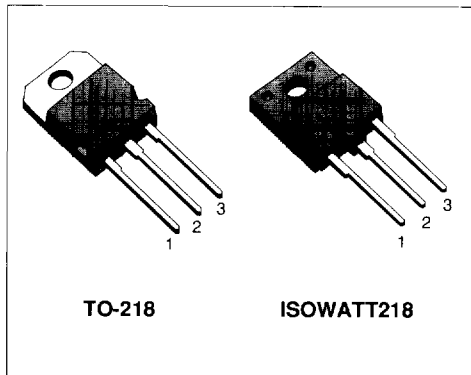
## N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTOR

TYPE	V <sub>DS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STH60N05	50 V	0.023 $\Omega$	60 A
STH60N05FI	50 V	0.023 $\Omega$	36 A

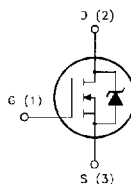
- AVALANCHE RUGGEDNESS TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE FOR STANDARD PACKAGE
- VERY LOW R<sub>DS(on)</sub>
- APPLICATION ORIENTED CHARACTERIZATION
- ISOLATED PACKAGE UL RECOGNIZED, ISOLATION TO 4000V DC

### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)



### INTERNAL SCHEMATIC DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STH60N05	STH60N05FI	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	50		V
V <sub>DGR</sub>	Drain- gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ )	50		V
V <sub>GS</sub>	Gate-source Voltage	$\pm 20$		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25 °C(■)	60	36	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100 °C	45	22	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	240	240	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25 °C	180	60	W
	Derating Factor	1.2	0.48	W/°C
T <sub>stg</sub>	Storage Temperature	-65 to 175	-65 to 150	°C
T <sub>J</sub>	Max. Operating Junction Temperature	175	150	°C

(●) Pulse width limited by safe operating area  
 (■) T<sub>C</sub> = 50 °C for TO-218

## THERMAL DATA

			TO-218	ISOWATT218	
$R_{th(case)}$	Thermal Resistance Junction-case	Max	0.83	2.08	$^{\circ}\text{C}/\text{W}$
$R_{th(amb)}$	Thermal Resistance Junction-ambient	Max	30		$^{\circ}\text{C}/\text{W}$
$R_{th(sink)}$	Thermal Resistance Case-sink	Typ	0.1		$^{\circ}\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose		300		$^{\circ}\text{C}$

## AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_l$ max, $\delta < 1\%$ )	60	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_l = 25^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 25\text{ V}$ )	700	mJ
$E_{AR}$	Repetitive Avalanche Energy (pulse width limited by $T_l$ max, $\delta < 1\%$ )	170	mJ
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive ( $T_c = 100^{\circ}\text{C}$ , pulse width limited by $T_l$ max, $\delta < 1\%$ )	36	A

ELECTRICAL CHARACTERISTICS ( $T_{case} = 25^{\circ}\text{C}$  unless otherwise specified)

## OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	50			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125^{\circ}\text{C}$			250 1000	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}$ $I_D = 30\text{ A}$ $T_c = 100^{\circ}\text{C}$			0.023 0.046	$\Omega$ $\Omega$
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	60			A

## DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 30\text{ A}$	16			S
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		2500	3000	pF
$C_{oss}$	Output Capacitance			950	1200	pF
$C_{rss}$	Reverse Transfer Capacitance			250	350	pF

# ELECTRICAL CHARACTERISTICS (continued)

## SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 40\text{ V}$ $I_D = 60\text{ A}$		120	160	ns
$t_r$	Rise Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		320	430	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 40\text{ V}$ $I_D = 60\text{ A}$ $R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 5)		160		A/ $\mu$ s
$Q_g$	Total Gate Charge	$V_{DD} = 25\text{ V}$ $I_D = 30\text{ A}$ $V_{GS} = 10\text{ V}$		65	90	nC

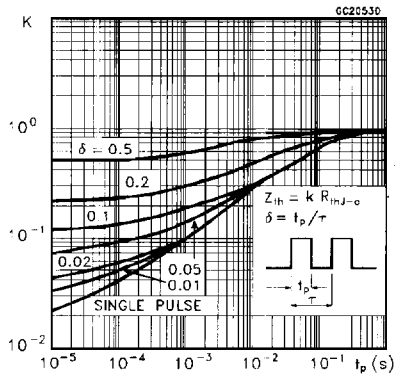
## SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Volt)}$	Off-voltage Rise Time	$V_{DD} = 40\text{ V}$ $I_D = 60\text{ A}$		170	230	ns
$t_f$	Fall Time	$R_G = 50\ \Omega$ $V_{GS} = 10\text{ V}$		170	230	ns
$t_c$	Cross-over Time	(see test circuit, figure 5)		340	460	ns

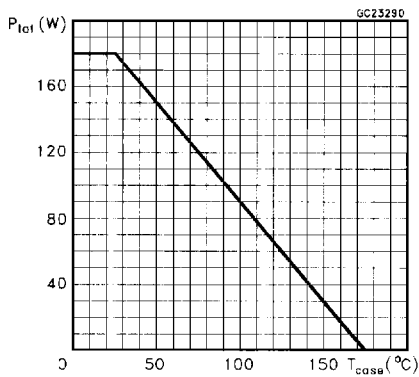
## SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				60	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				240	A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 60\text{ A}$ $V_{GS} = 0$			1.7	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 60\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 5)		120		ns
$Q_{rr}$	Reverse Recovery Charge			0.25		$\mu\text{C}$
$I_{RRM}$	Reverse Recovery			5		A

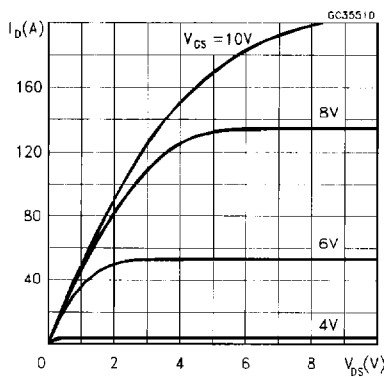
Thermal Impedance For TO-218



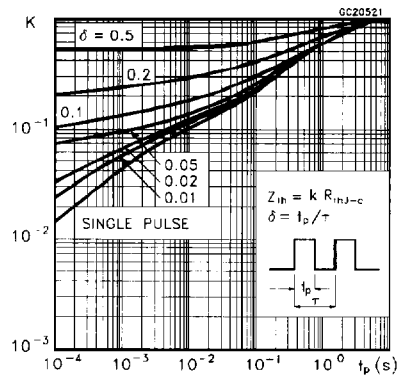
Derating Curve For TO-218



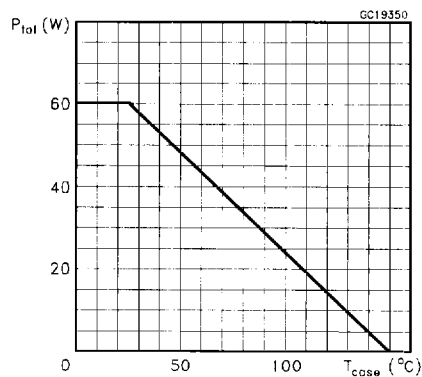
Output Characteristics



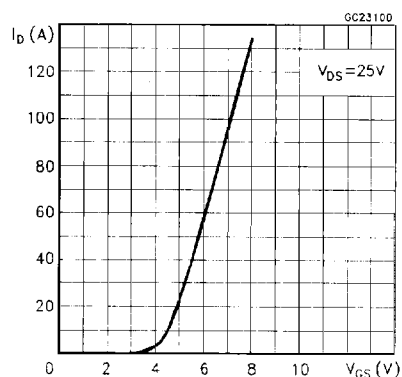
Thermal Impedance For ISOWATT218



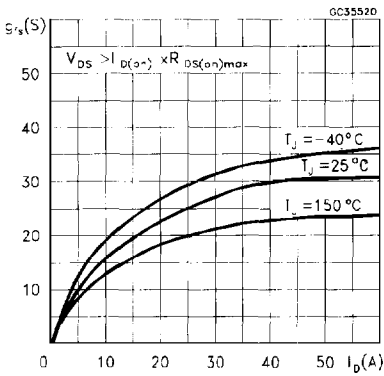
Derating Curve For ISOWATT218



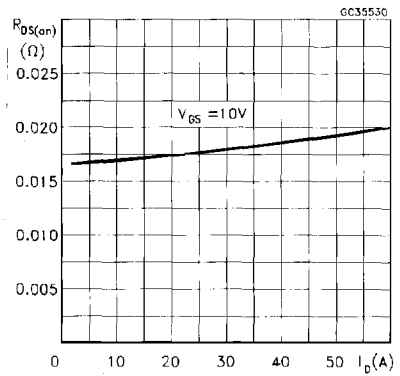
Transfer Characteristics



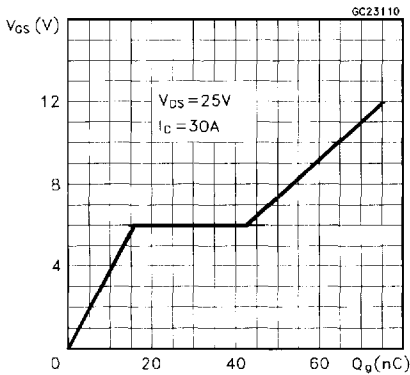
## Transconductance



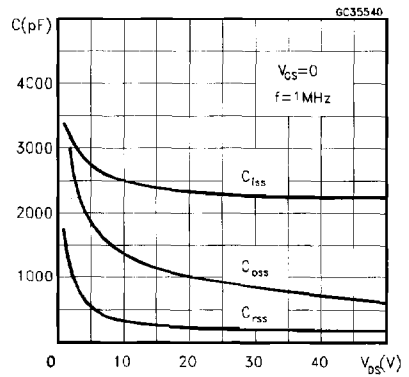
## Static Drain-source On Resistance



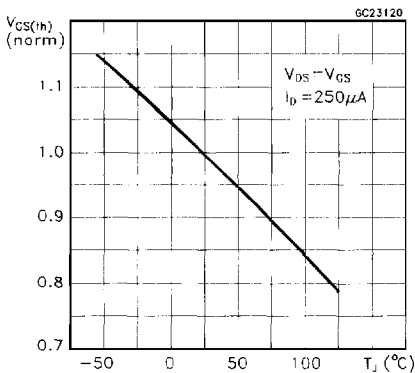
## Gate Charge vs Gate-source Voltage



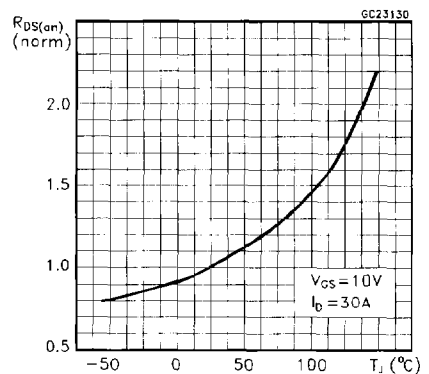
## Capacitance Variations



## Normalized Gate Threshold Voltage vs Temperature



## Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

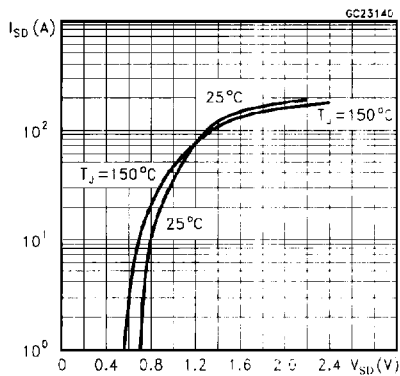


Fig. 2: Unclamped Inductive Waveforms

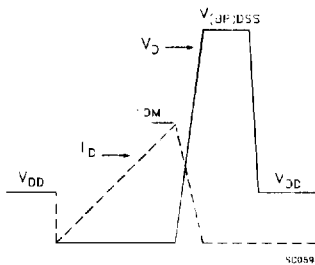


Fig. 4: Gate Charge Test Circuit

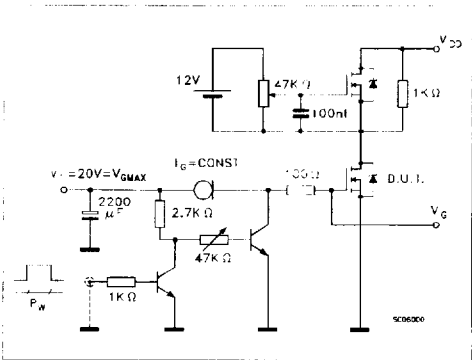


Fig. 1: Unclamped Inductive Load Test Circuits

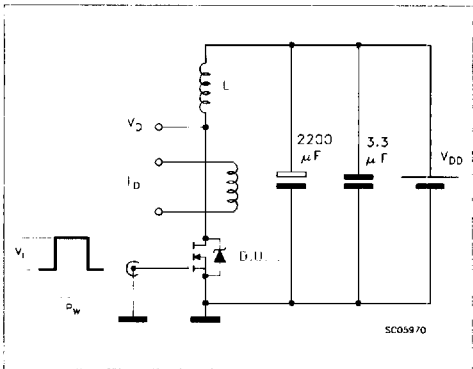


Fig. 3: Switching Times Test Circuits For Resistive Load

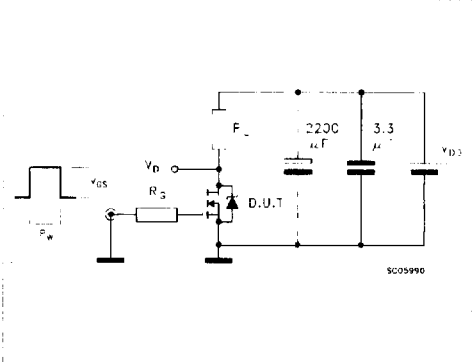


Fig. 5: Test Circuit For Inductive Load Switching And Diode Reverse Recovery Time

