

## 2A BUS TERMINATION REGULATOR

### Description

The FP6137E linear regulator is designed to provide the transient peaks up to 2A sourcing or sinking capability for DDR SDRAM bus termination application. The output voltage can track half of input power by two external voltage divider resistors.

The FP6137E provides current limiting in both sourcing/sinking mode and thermal shutdown function which protects the excessive heating due to high current and high junction temperature.

The FP6137E is available in the SOP-8 (Exposed Pad) package.

### Features

- 2A Source or Sink Current
- Power MOSFET Integrated
- Low Output Voltage Offset
- Current Limiting Protection
- Thermal Shutdown Protection
- Adjusted Output by External Resistors
- Shutdown for Standby or Suspend Mode
- RoHS Compliant

### Applications

- DDR-I, DDR-II, and DDR-III Bus Termination Voltage
- SSTL-2 and SSTL-3 Termination
- Active Termination Buses

### Pin Assignments

SP Package (SOP-8<Exposed Pad>)

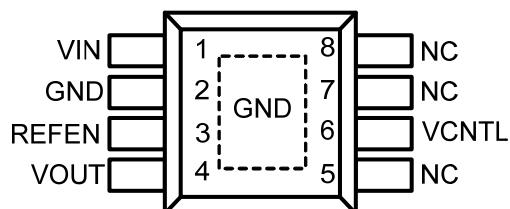
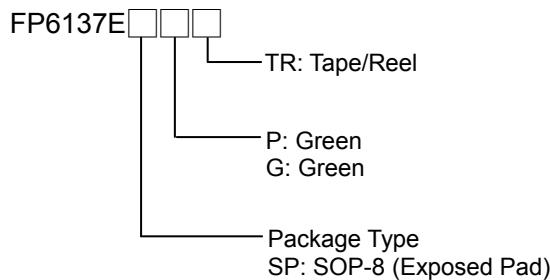


Figure 1. Pin Assignment of FP6137E (Top View)

### Ordering Information



## Typical Application Circuit

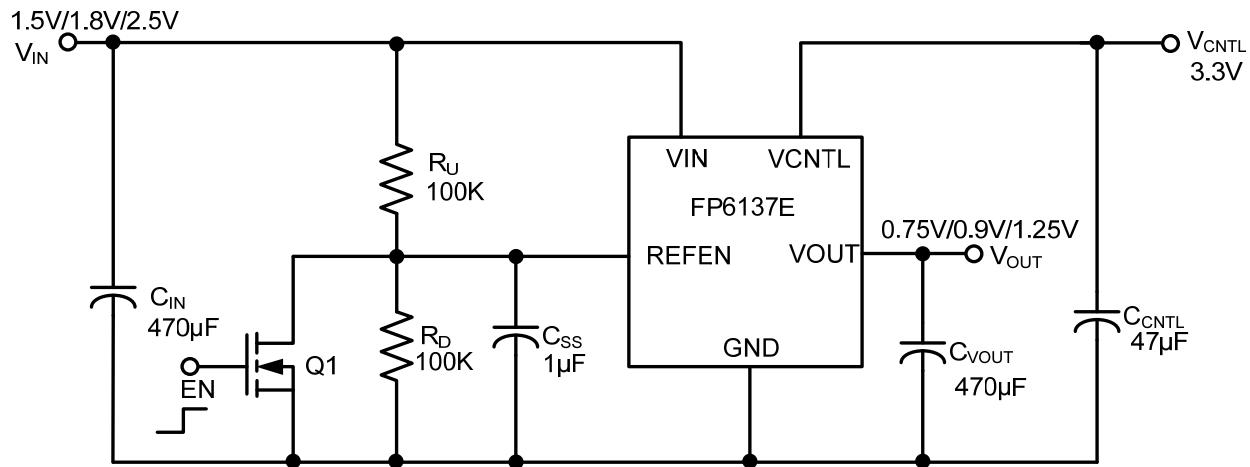


Figure 2. Typical Application Circuit of FP6137E

## Functional Pin Description

Pin Name	Pin Function
<b>VIN</b>	Power input pin. VIN is the input power supply used to create the external reference voltage for regulating VOUT. VIN sources current to VOUT by upper NMOS.
<b>GND</b>	Common ground pin. The VOUT sinks current to GND by lower NMOS.
<b>VCNTL</b>	Power input pin. The VCNTL power supplies the internal control circuitry and gate drive voltage.
<b>REFEN</b>	Chip enable, and input reference voltage pin. The reference voltage is half of the VIN power by two external voltage divide resistors.
<b>VOUT</b>	Regulator output pin. VOUT voltage tracks the REFEN voltage and is capable of sourcing or sinking current up to peak 2A.

## Block Diagram

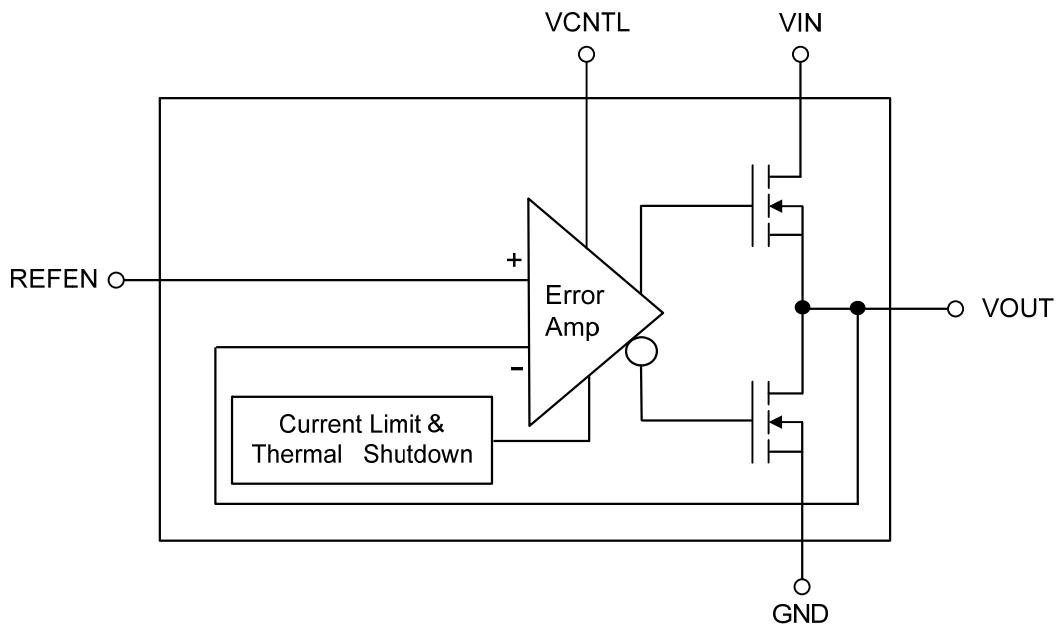


Figure 3. Block Diagram of FP6137E

## Absolute Maximum Ratings

• VIN to GND -----	6V
• VCNTL to GND -----	6V
• Power Dissipation @25°C ( $P_D$ ) SOP-8 (Exposed Pad) -----	1.25W
• Package Thermal Resistance ( $\theta_{JA}$ ) SOP-8 (Exposed Pad) -----	80°C/W
• Junction Temperature -----	150°C
• Storage Temperature Range-----	-65°C to 150°C
• Lead Temperature (Soldering, 10sec.) -----	260°C
• ESD Susceptibility HBM(Human Body Mode) -----	2KV
MM(Machine Mode) -----	200V

Note1 : Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

## Recommended Operating Conditions

• Input Voltage ( $V_{IN}$ ) -----	1.5V, 1.8V or 2.5V
• Input Voltage ( $V_{CNTL}$ ) -----	3.3V to 5.5V
• Operating Temperature Range ( $T_{OPR}$ ) -----	- 40°C to + 85°C



## Electrical Characteristics

( $V_{CNTL}=3.3V$ ,  $V_{IN}=1.5V/1.8V/2.5V$ ,  $V_{REFEN}=0.5*V_{IN}$ ,  $C_{OUT}=10\mu F$ ,  $T_A=25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>INPUT</b>						
Operation Voltage Range (DDRI /DDII/ DDR-III)	$V_{CNTL}$			3.3	5.5	V
$V_{CNTL}$ Quiescent Current	$I_{CNTL}$	No Load		1.5	3.0	mA
Shutdown Current	$I_{SD}$	$V_{REFEN}<0.2V$		5	30	$\mu A$
<b>OUTPUT VOLTAGE</b>						
Output Offset Voltage	$V_{OS}$	No Load , ( $V_{REFEN}-V_{OUT}$ )	-20	0	20	mV
Load Regulation (Note2) (DDRI/DDII/DDR-III)	$ \Delta V_{LOAD} $	$I_{OUT} = 0 \text{ to } 2A$			20	mV
		$I_{OUT} = 0 \text{ to } 2A$			20	
<b>PROTECTION</b>						
Current Limit	$I_{LIM}$		2.0	2.5		A
Thermal Shutdown Temperature (Note3)	$T_{SD}$			170		$^\circ C$
	$\Delta T_{SD}$	Hysteresis		35		$^\circ C$
<b>SHUTDOWN CONTROL</b>						
Enable High Level	$V_{REF-H}$		0.6			V
Shutdown Low Level	$V_{REF-L}$				0.2	V

Note2 : Load regulation is measured at a constant junction temperature by using a 20ms low duty cycle current pulse.

Note3 : Guarantee by design.

## Typical Performance Curves

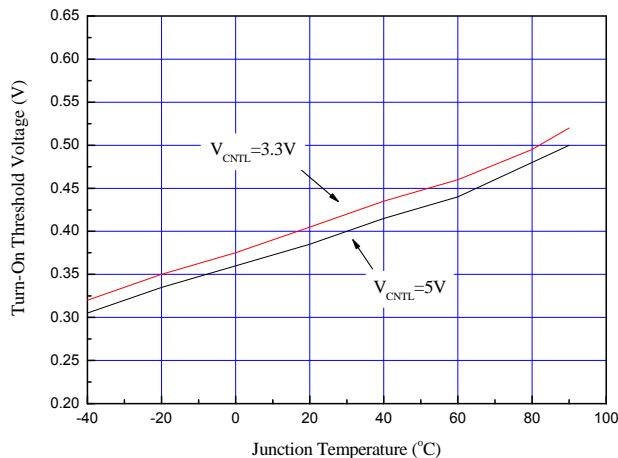


Figure 4. Turn-On Threshold Voltage vs. Junction Temperature

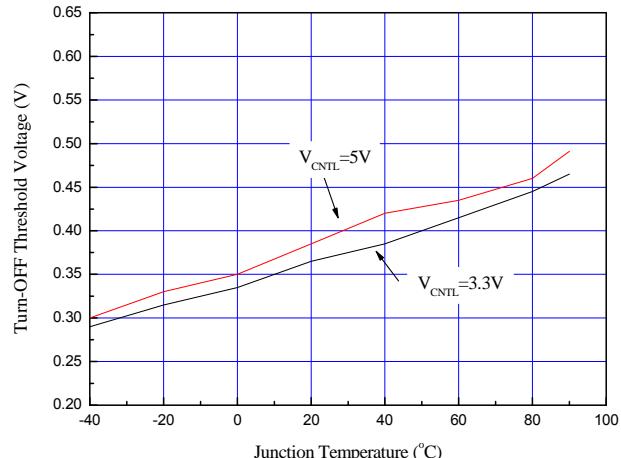


Figure 5. Turn-Off Threshold Voltage vs. Junction Temperature

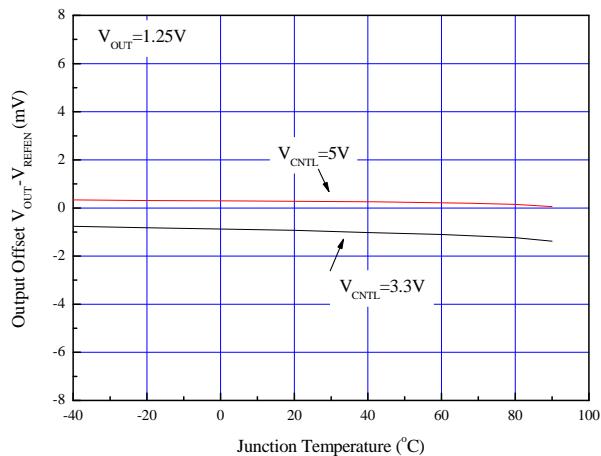


Figure 6. Output offset (V<sub>OUT</sub>-V<sub>REFEN</sub>) vs. Junction Temperature

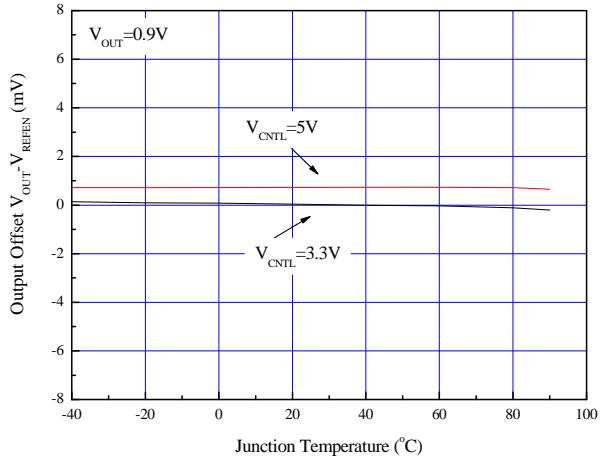


Figure 7. Output offset (V<sub>OUT</sub>-V<sub>REFEN</sub>) vs. Junction Temperature

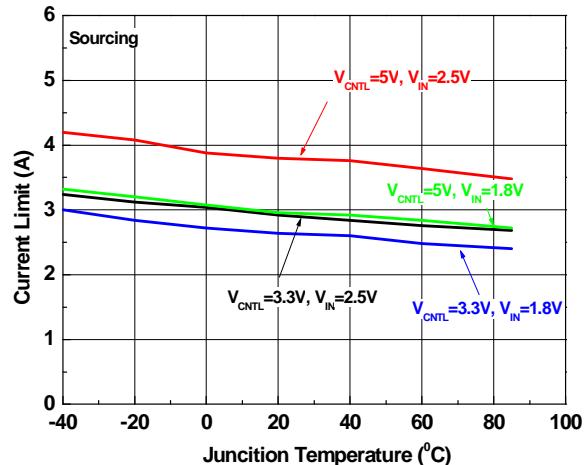


Figure 8. Current Limit vs. Junction Temperature

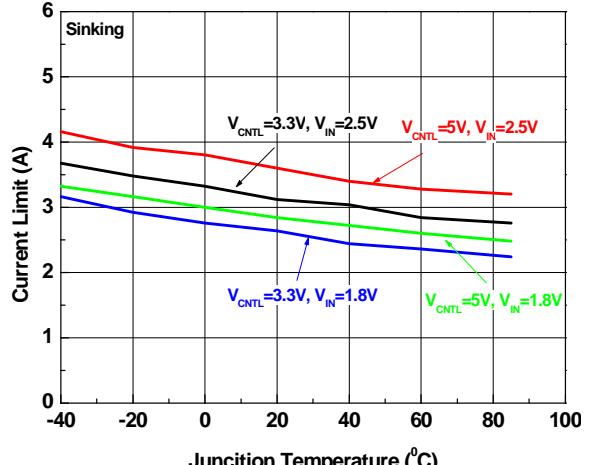


Figure 9. Current Limit vs. Junction Temperature

## Typical Performance Curves (Continued)

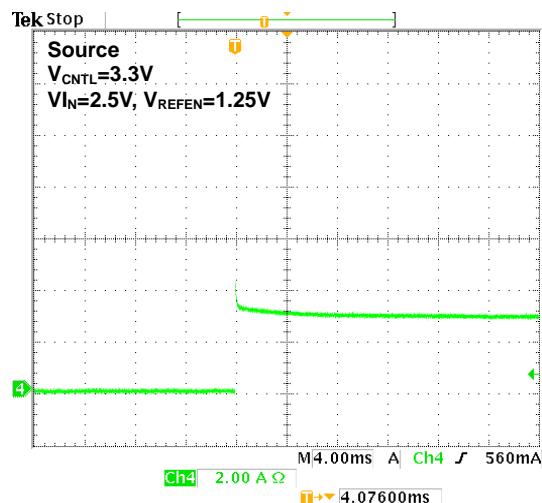


Figure10. Output Short-Circuit Protection

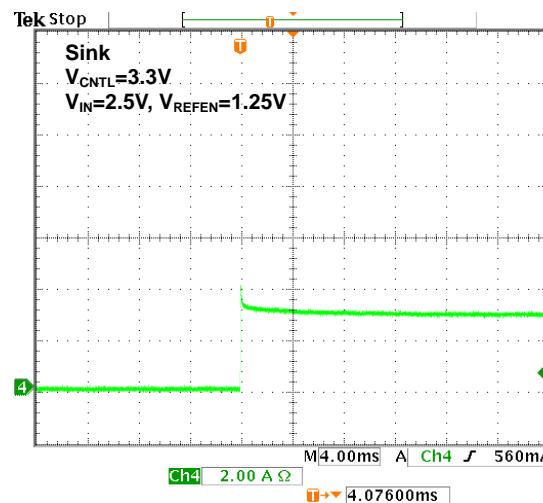


Figure11. Output Short-Circuit Protection

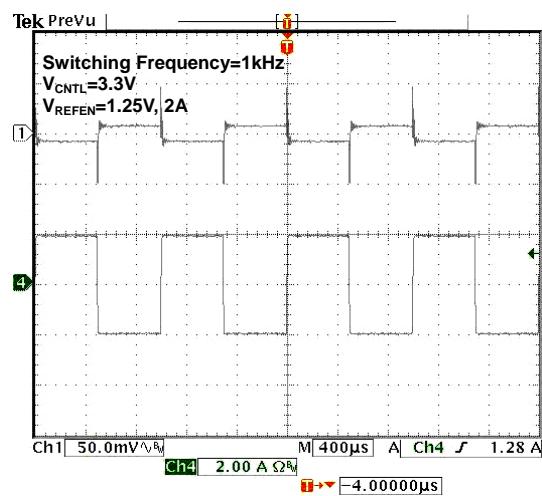


Figure12.  $1.25V_{OUT}$  @ 2A Transient Response

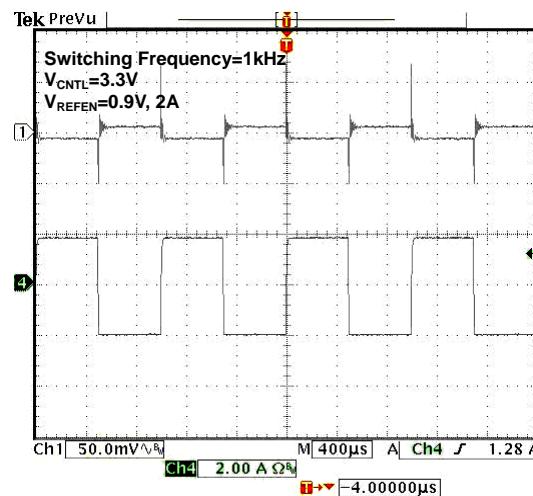
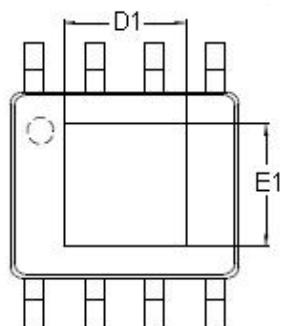
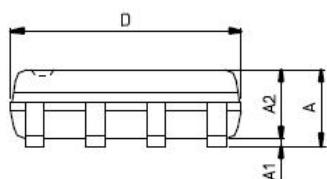
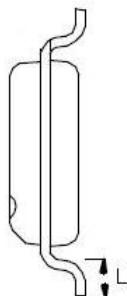
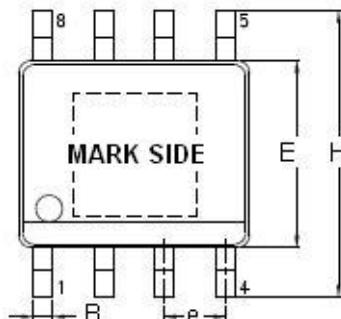


Figure13.  $0.9V_{OUT}$  @ 2A Transient Response

## Outline Information

**SOP- 8 (Exposed Pad) Package (Unit: mm)**



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	1.25	1.70
A1	0.00	0.15
A2	1.25	1.55
B	0.31	0.51
D	4.80	5.00
D1	1.82	3.35
E	3.80	4.00
E1	1.82	2.41
e	1.20	1.34
H	5.80	6.20
L	0.40	1.27

Note : Followed From JEDEC MO-012-E.

### Life Support Policy

Fitipower's products are not authorized for use as critical components in life support devices or other medical systems.