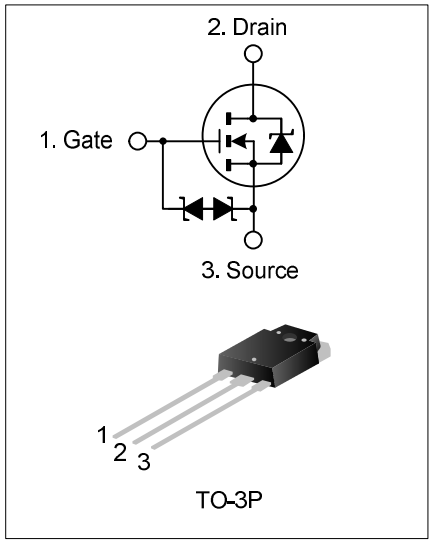
18A 500V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVF18NE50PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

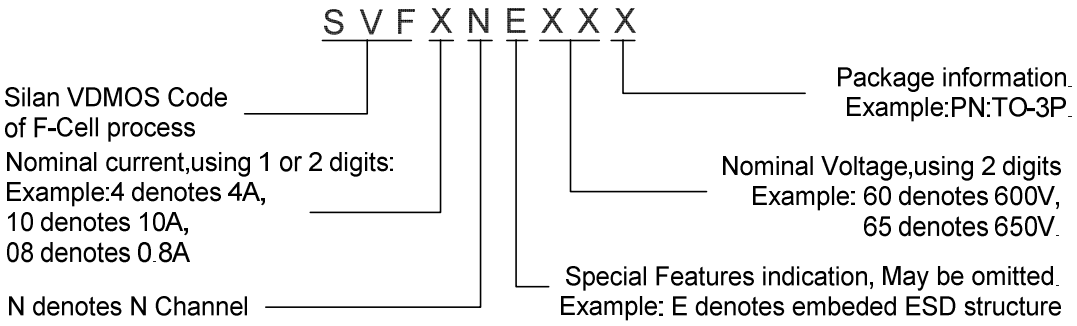
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

- 18A,500V,$R_{DS(on(typ))}$=0.26Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVF18NE50PN	TO-3P	18NE50	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	500	V
Gate-Source Voltage		V_{GS}	±30	V
Drain Current	T_C=25°C	I_D	18.0	A
	T_C=100°C		11.38	
Drain Current Pulsed		I_{DM}	72.0	A
Power Dissipation(T_C=25°C)		P_D	240	W
-Derate above 25°C			1.92	W/°C
Single Pulsed Avalanche Energy (Note 1)		E_{AS}	1515	mJ
Operation Junction Temperature Range		T_J	-55～+150	°C
Storage Temperature Range		T_{stg}	-55～+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.52	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	500	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±25V, V_{DS}=0V	--	--	±100	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=9.0A	--	0.26	0.31	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	2265.4	--	pF
Output Capacitance	C_{oss}		--	280.2	--	
Reverse Transfer Capacitance	C_{rss}		--	10.8	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=250V,I_D=18.0A, R_G=25Ω (Note 2,3)	--	36.64	--	ns
Turn-on Rise Time	t_r		--	60.52	--	
Turn-off Delay Time	$t_{d(off)}$		--	124.60	--	
Turn-off Fall Time	t_f		--	55.44	--	
Total Gate Charge	Q_g	V_{DS}=400V,I_D=18.0A, V_{GS}=10V (Note 2,3)	--	44.51	--	nC
Gate-Source Charge	Q_{gs}		--	11.59	--	
Gate-Drain Charge	Q_{gd}		--	16.09	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode	--	--	18.0	A
Pulsed Source Current	I_{SM}	in the MOSFET	--	--	72.0	
Diode Forward Voltage	V_{SD}	I_S=18.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=18.0A,V_{GS}=0V,	--	546.33	--	ns
Reverse Recovery Charge	Q_{rr}	dI_F/dt=100A/μs(Note 2)	--	6.16	--	μC

Notes:

1. L=30mH, I_{AS}=10A,V_{DD}=100V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

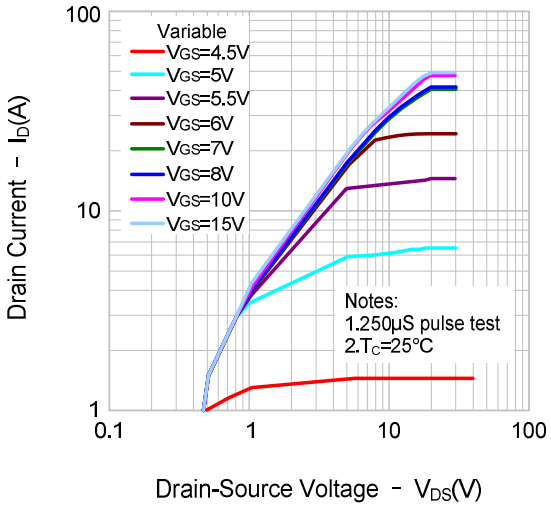


Figure 2. Transfer Characteristics

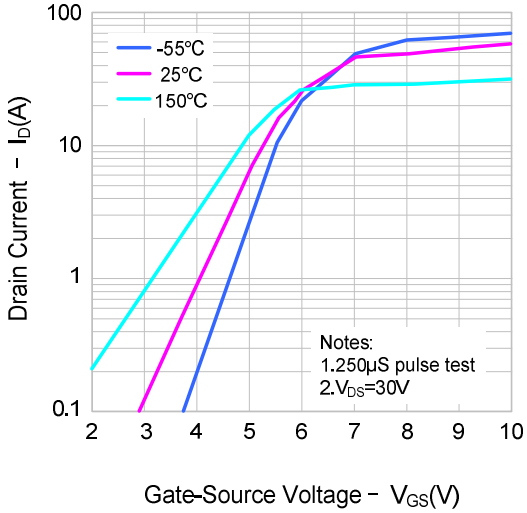


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

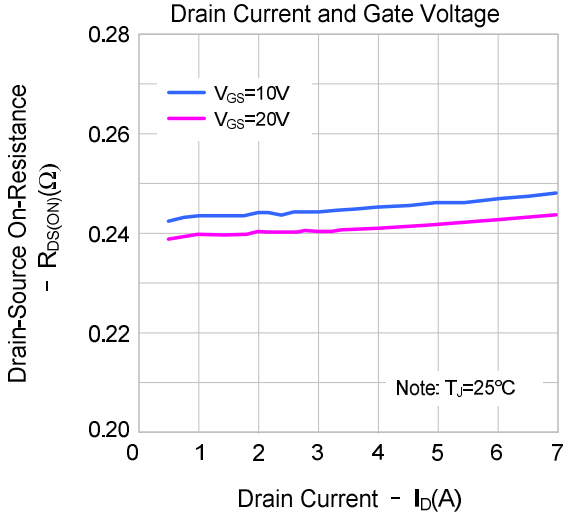
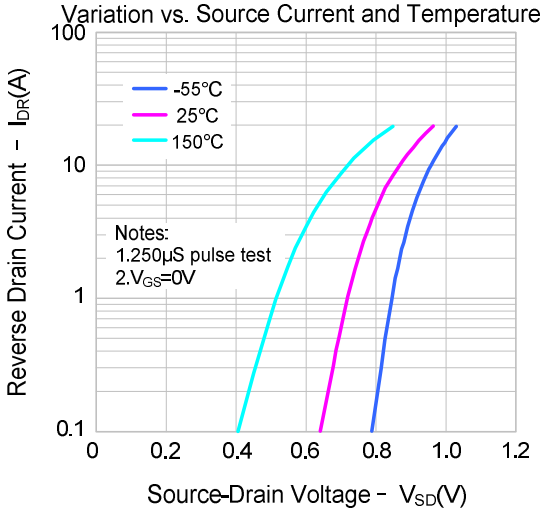


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Capacitance Characteristics

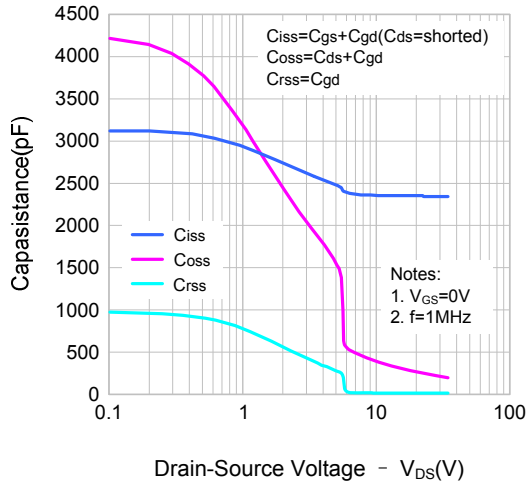


Figure 6. Gate Charge Characteristics

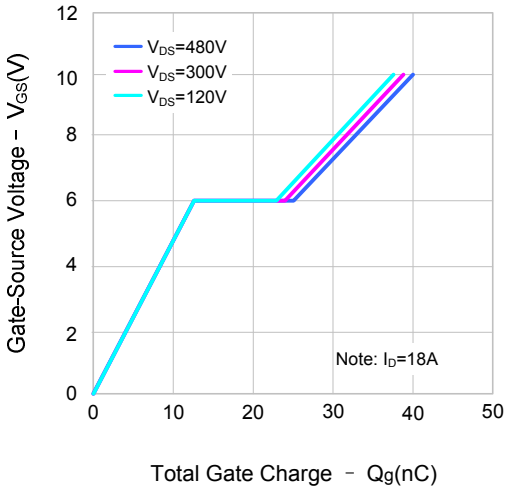


Figure 7. Breakdown Voltage Variation vs. Temperature

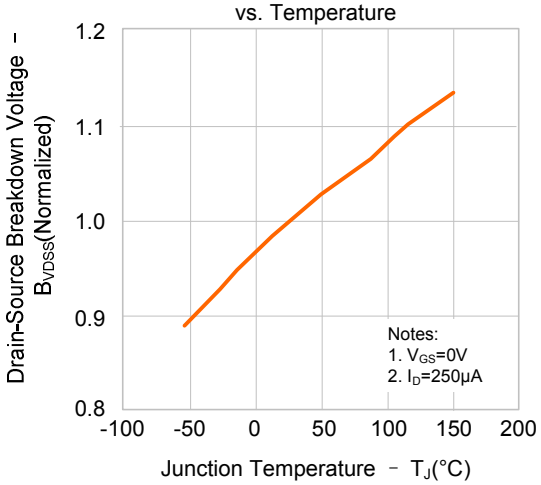


Figure 8. On-resistance Variation vs. Temperature

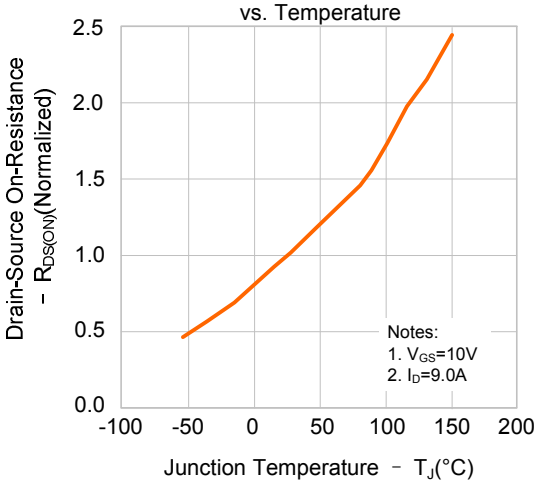


Figure 9. Max. Safe Operating Area

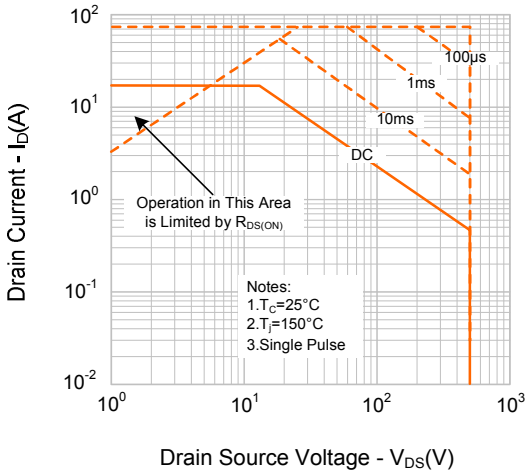
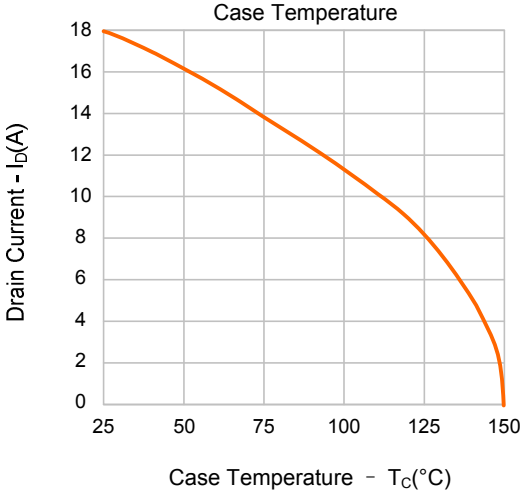
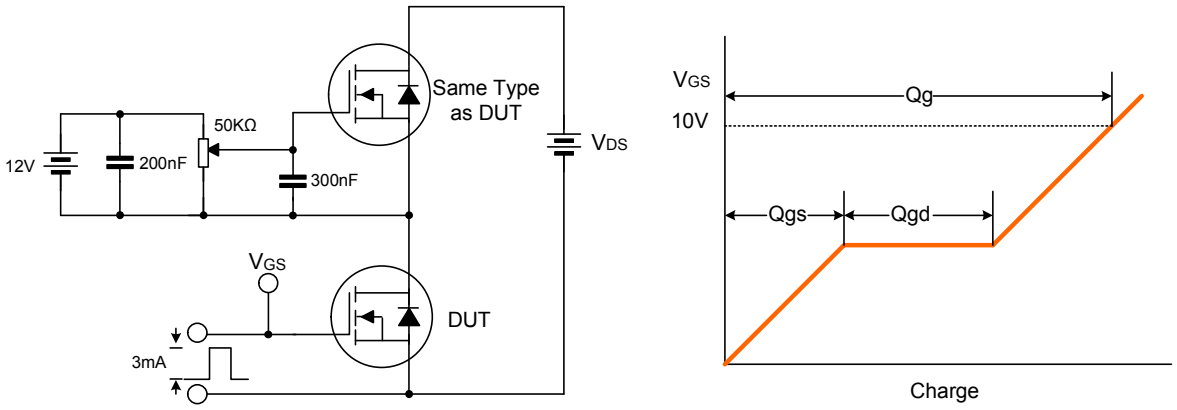


Figure 10. Maximum Drain Current vs. Case Temperature

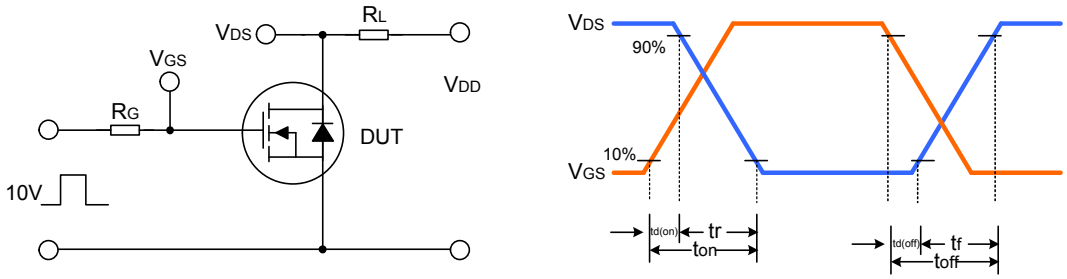


TYPICAL TEST CIRCUIT

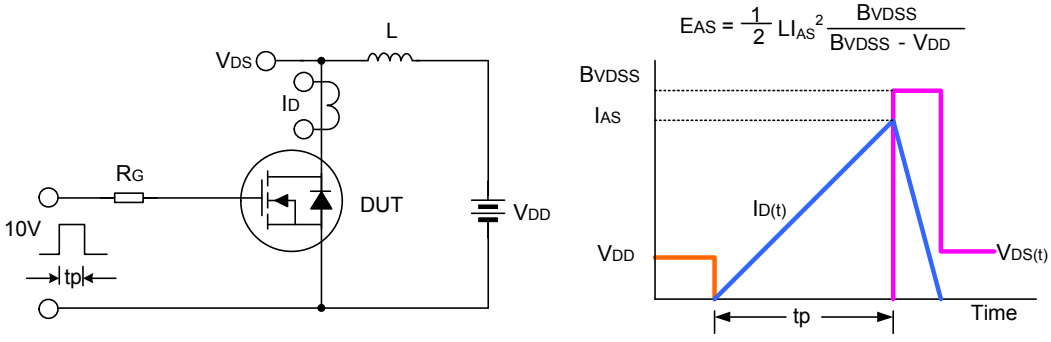
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

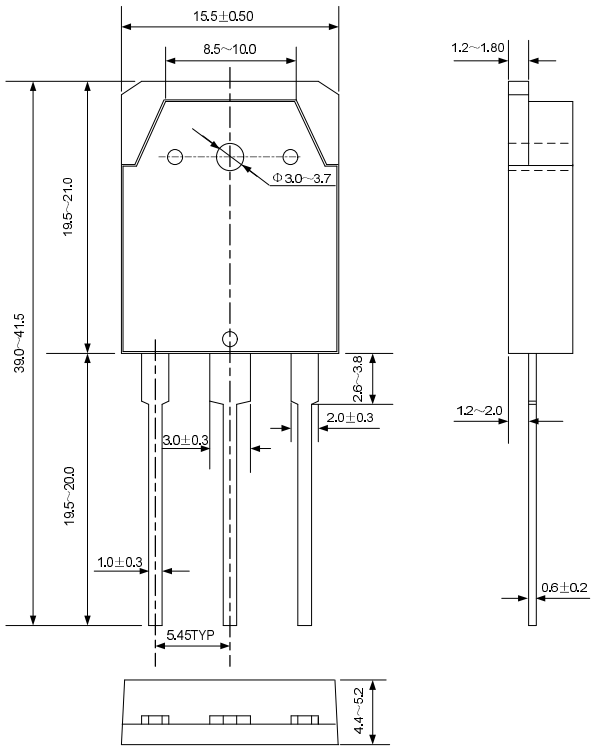


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-3P **UNIT: mm**



Disclaimer :

- **Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.**
- **All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.**
- **Silan will supply the best possible product for customers!**

Part No.:	SVF18NE50PN	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http: //www.silan.com.cn

Rev.:	1.0	Author:	Yin Zi

Revision History:

1. First release