N-Channel Enhancement MOSFET

GENERAL DESCRIPTION

The ME25N06 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 62m\Omega$ @VGS=10V
- $R_{DS(ON)} \leqq 86m\Omega$ @VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

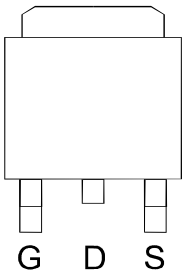
APPLICATIONS

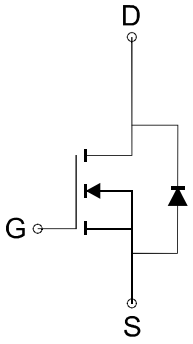
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252)

Top View





N-Channel MOSFET

Ordering Information: ME25N06 (Pb-free)

ME25N06-G (Green product)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	60		V
Gate-Source Voltage		V_{GSS}	±25		V
Continuous Drain Current(Tj=150℃)	T_C=25℃	I_D	16		A
	T_C=70℃		13		
Pulsed Drain Current		I_{DM}	65		A
Maximum Power Dissipation	T_C=25℃	P_D	25		W
	T_C=70℃		16		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	Steady State	5	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel Enhancement MOSFET

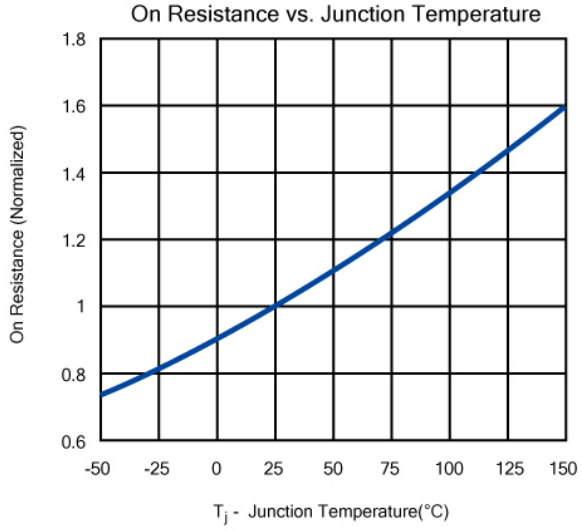
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V,T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 15A		52	62	mΩ
		V_{GS}=4.5V, I_D= 10A		70	86	
V_{SD}	Diode Forward Voltage	I_S=15A, V_{GS}=0V		1		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=48V, V_{GS}=10V, I_D=16A		17		nC
Qgs	Gate-Source Charge			4.2		
Qgd	Gate-Drain Charge			5		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.6		Ω
Ciss	Input Capacitance	V_{DS}=30V, V_{GS}=0V, f=1MHz		523		pF
Coss	Output Capacitance			47		
Crss	Reverse Transfer Capacitance			14		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L =15Ω I_D=1A, V_{GEN}=10V R_G=3Ω		11		ns
tr	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			34		
tf	Turn-Off Fall Time			4		

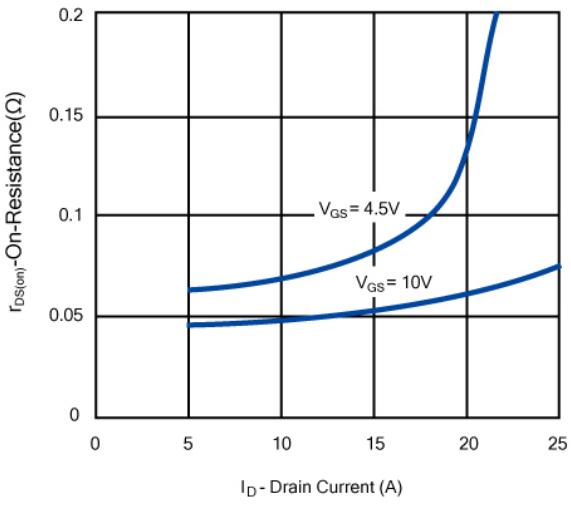
Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

Typical Characteristics (T_J =25℃ Noted)

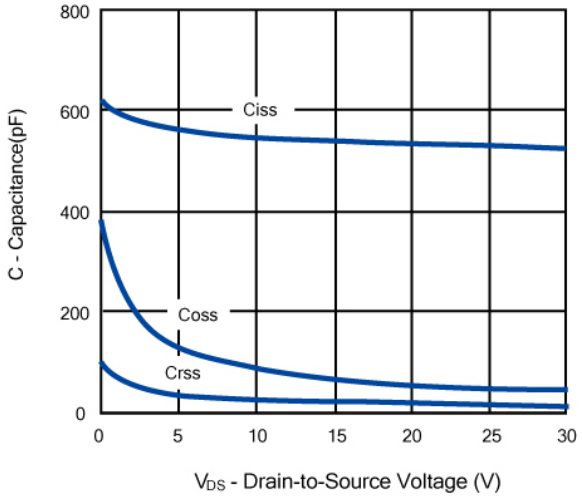
On Resistance vs. Junction Temperature



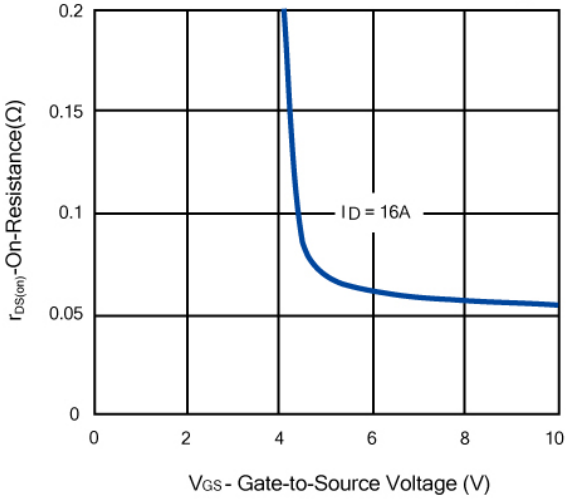
On-Resistance vs. Drain Current



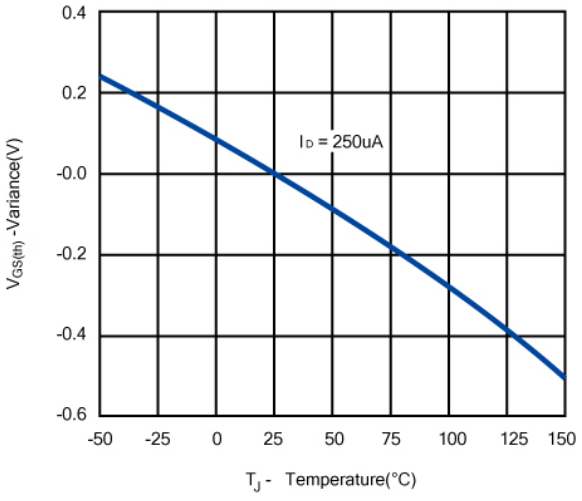
Capacitance



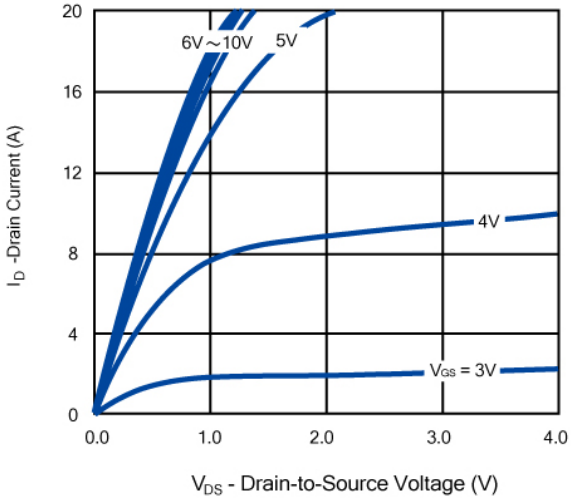
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

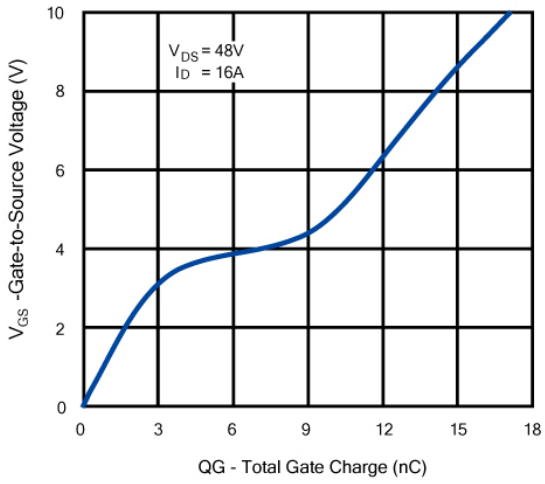


On-Region Characteristics

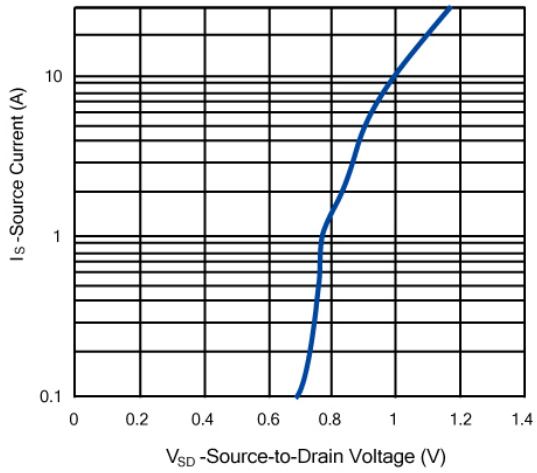


Typical Characteristics (T_J =25℃ Noted)

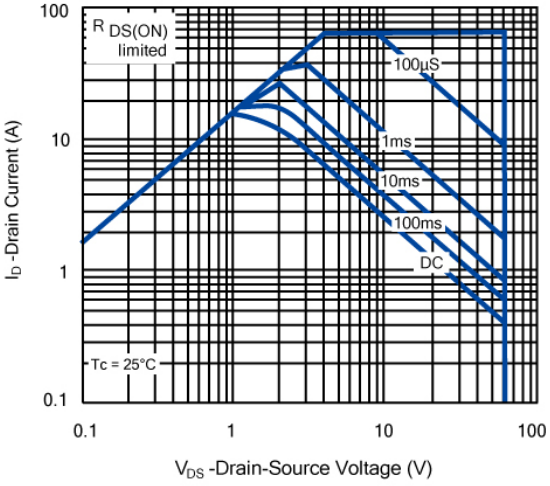
Gate Charge



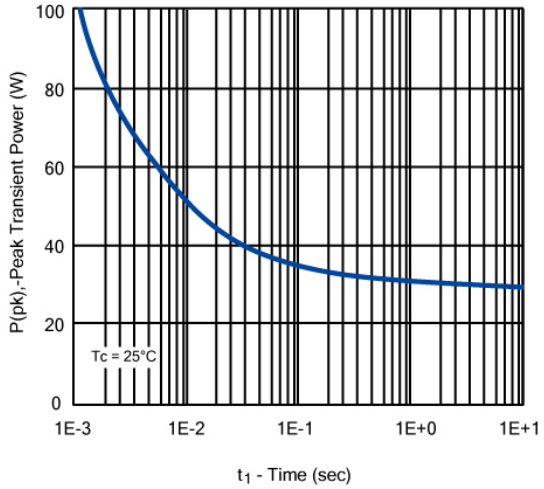
On-Resistance vs. Drain Current



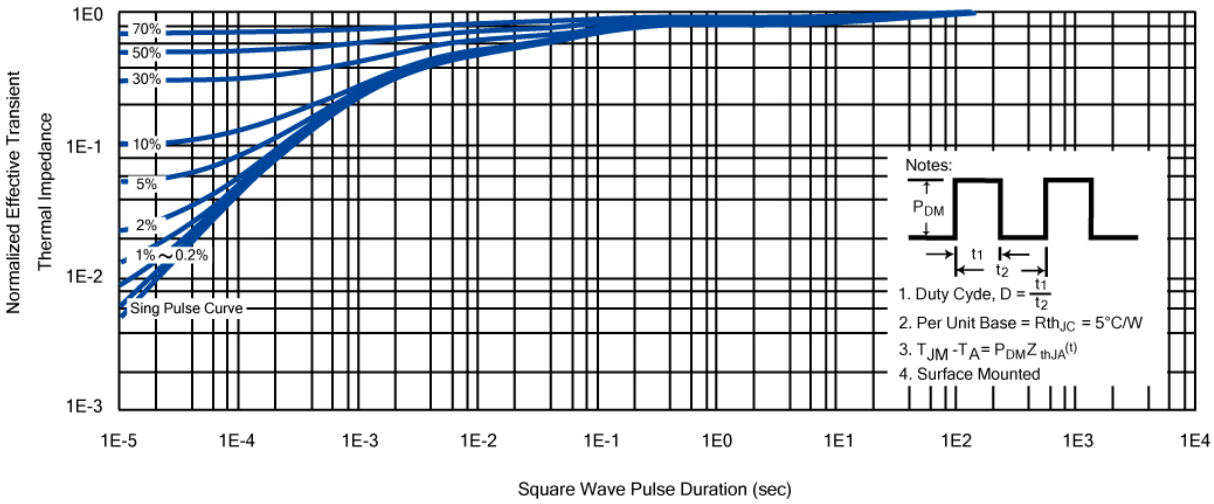
Maximum Forward Biased Safe Operating Area



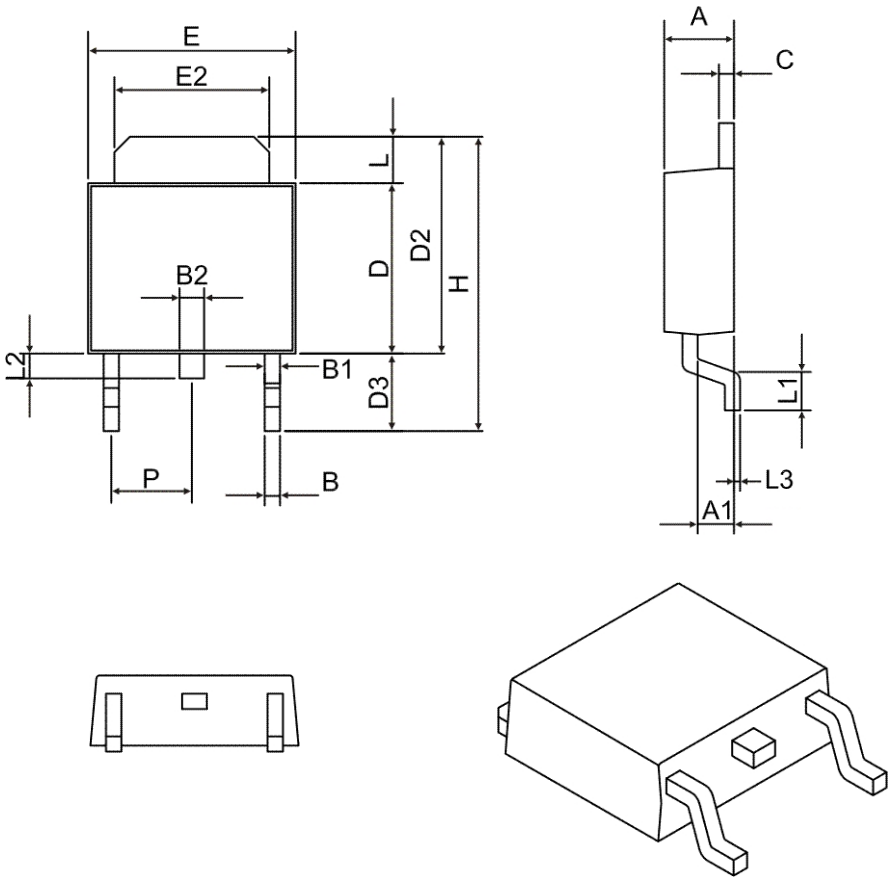
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



TO-252 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.90	1.30
B	0.50	0.85
B1	0.50	0.80
B2	0.50	1.00
C	0.40	0.60
D	5.20	5.70
D2	6.50	7.30
D3	2.20	3.00
H	9.50	10.50
E	6.30	6.80
E2	4.50	5.50
L	1.30	1.70
L1	0.90	1.70
L2	0.50	1.10
L3	0	0.30
P	2.00	2.80