P- Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME45P04-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 18m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 25m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

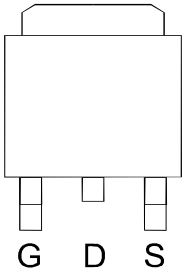
APPLICATIONS

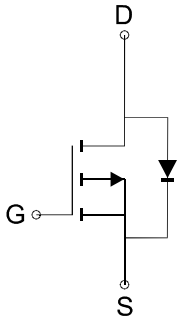
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252)

Top View





P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating		Unit
Drain-Source Voltage		V_{DSS}	-40		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(Tj=150℃)*	T_C=25℃	I_D	-30		A
	T_C=70℃		-23		
Pulsed Drain Current		I_{DM}	-100		A
Maximum Power Dissipation*	T_C=25℃	P_D	25		W
	T_C=70℃		16		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Typ	40	℃/W
			Max	50	
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	5		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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P- Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.5	-1.8	-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-40V, V_{GS}=0V			1	μA
		V_{DS}=-40V, V_{GS}=0V,T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -12A		15	18	mΩ
		V_{GS}=-4.5V, I_D= -6A		18	25	
V_{SD}	Diode Forward Voltage	I_S=-1.7A, V_{GS}=0V		0.78	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-20V, V_{GS}=-4.5V, I_D=-12A		25	33	nC
Qgs	Gate-Source Charge			11		
Qgd	Gate-Drain Charge			9.5		
Rg	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		8.5		Ω
Ciss	Input capacitance	V_{DS}=-20V, V_{GS}=0V, F=1MHz		2760	3726	pF
Coss	Output Capacitance			260		
Crss	Reverse Transfer Capacitance			85		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V, R_G=6Ω		48	64	ns
t_r	Turn-On Rise Time			24	32	
$t_{d(off)}$	Turn-Off Delay Time			88	118	
t_f	Turn-On Fall Time			34	45	

Notes:a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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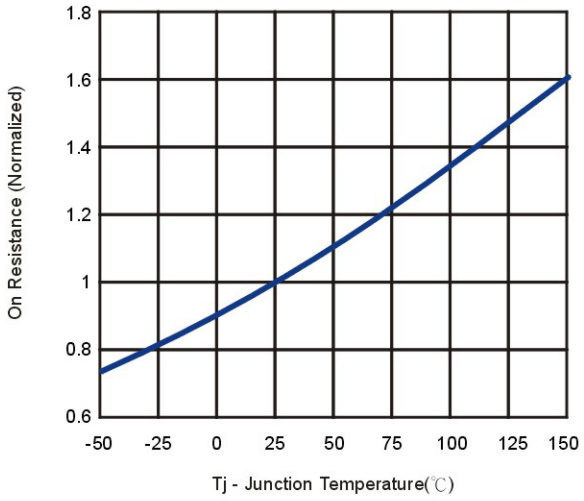
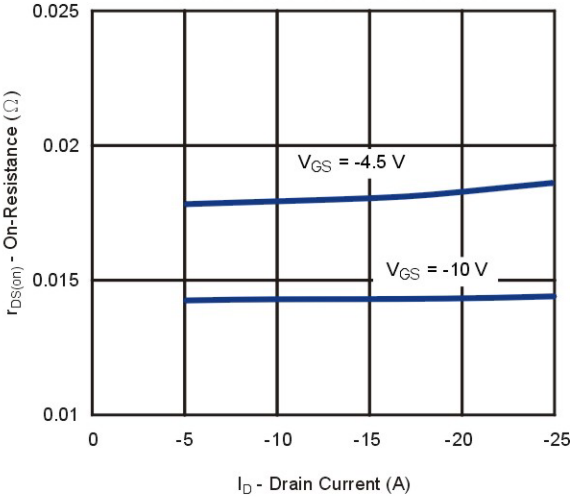
P- Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

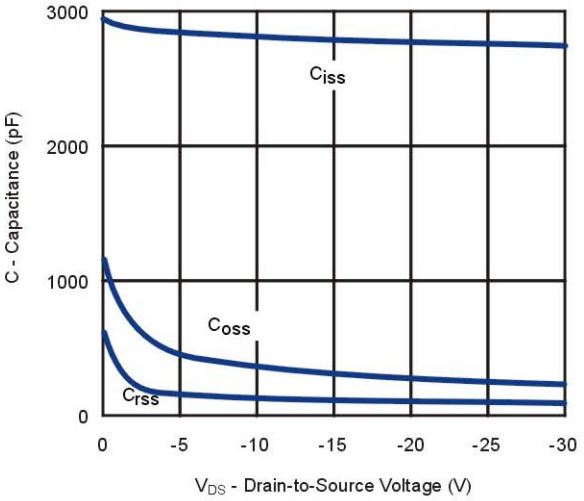
On Resistance vs. Junction Temperature



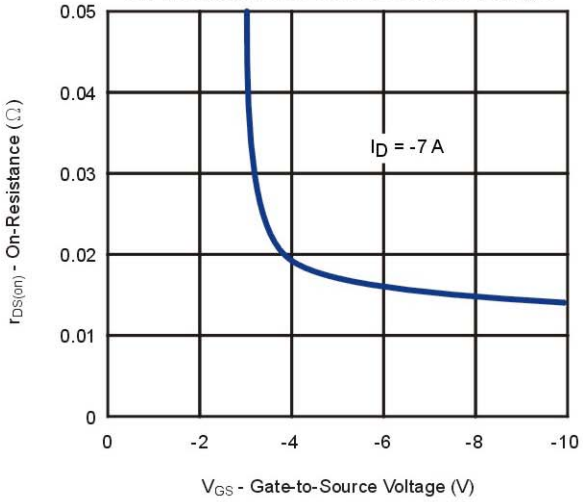
On-Resistance vs. Drain Current



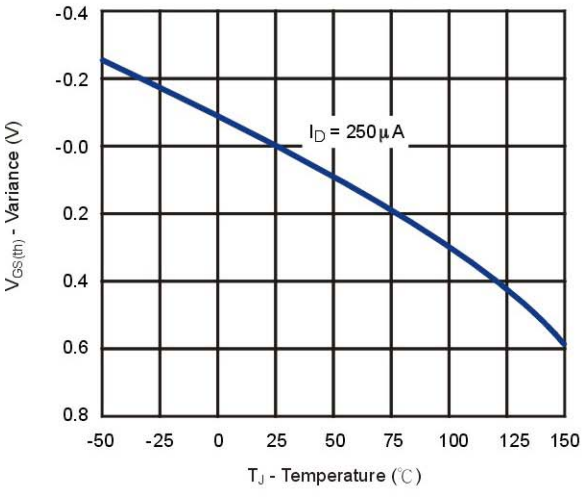
Capacitance



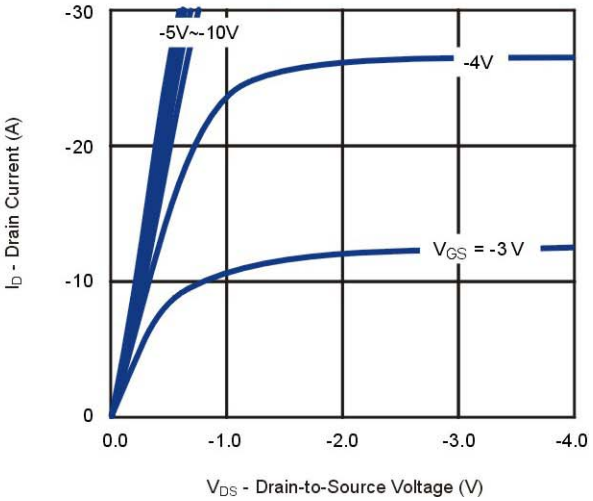
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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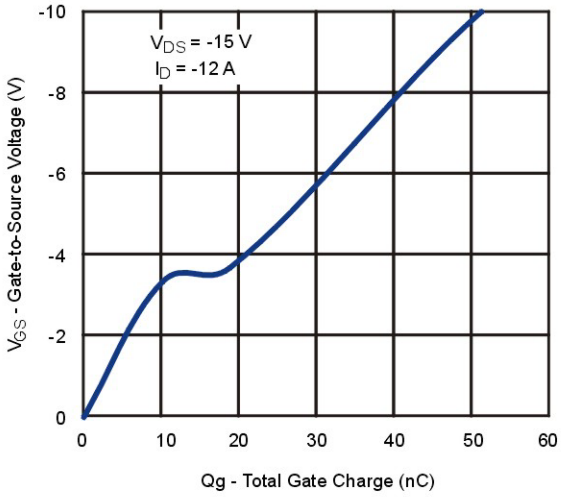
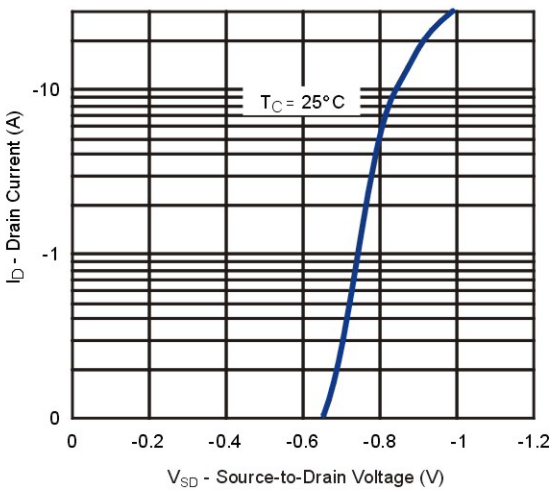
Typical Characteristics (T_J =25℃ Noted)

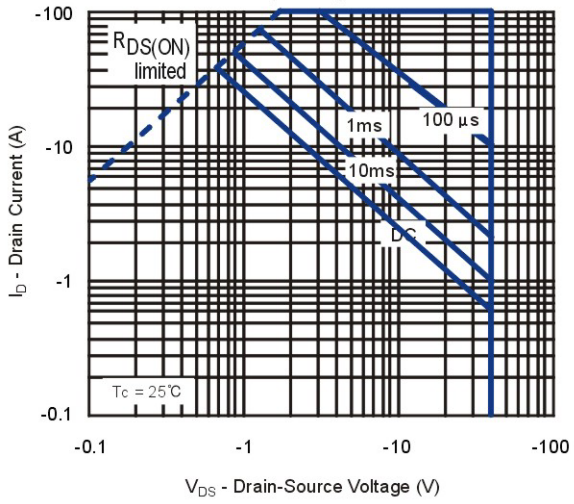
Gate Charge



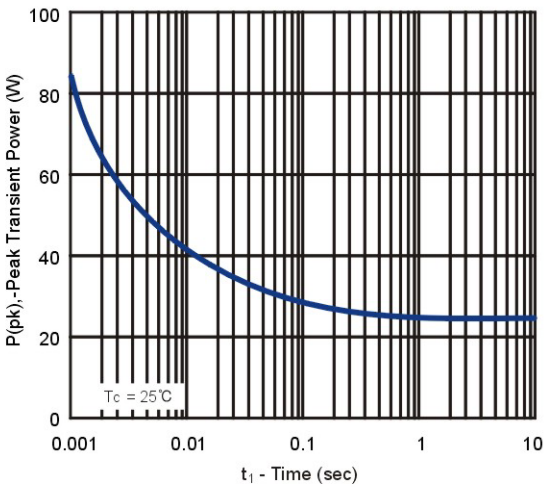
On-Resistance vs. Drain Current



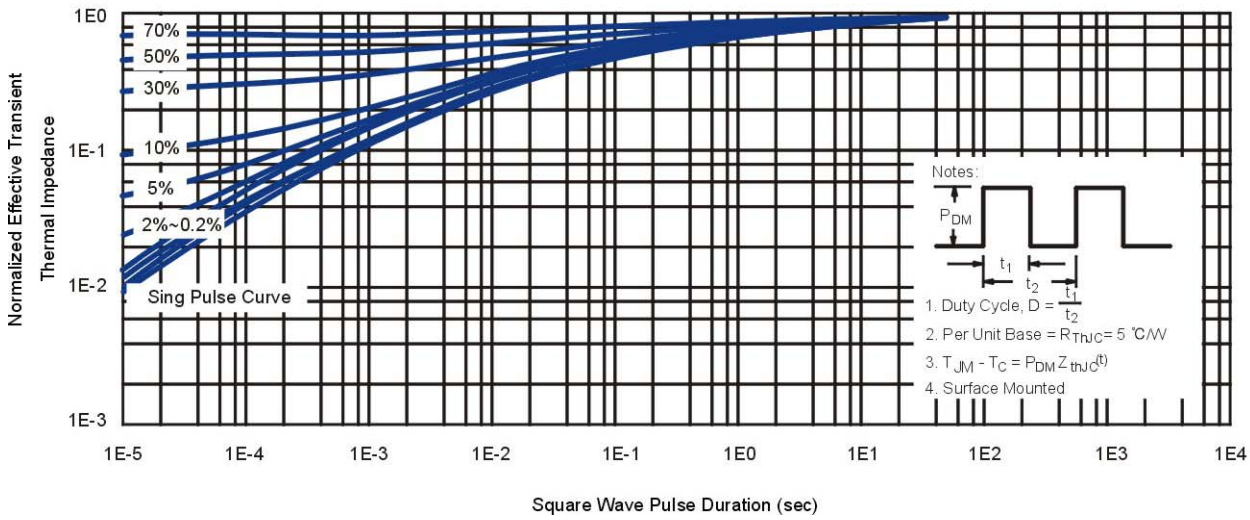
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Case



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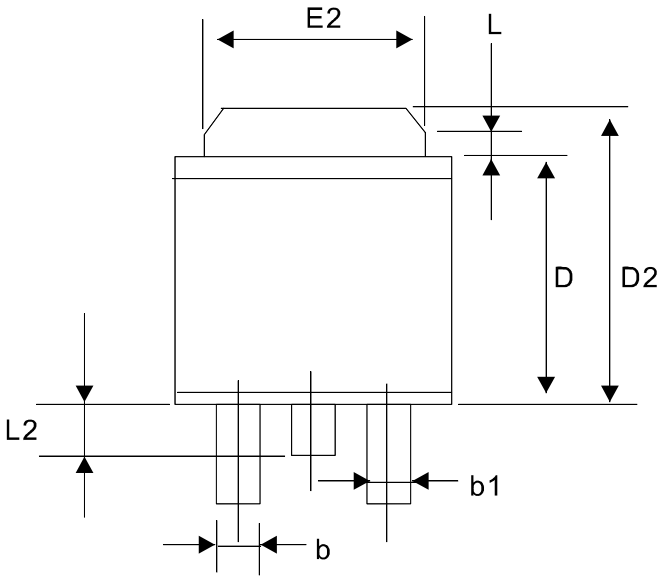
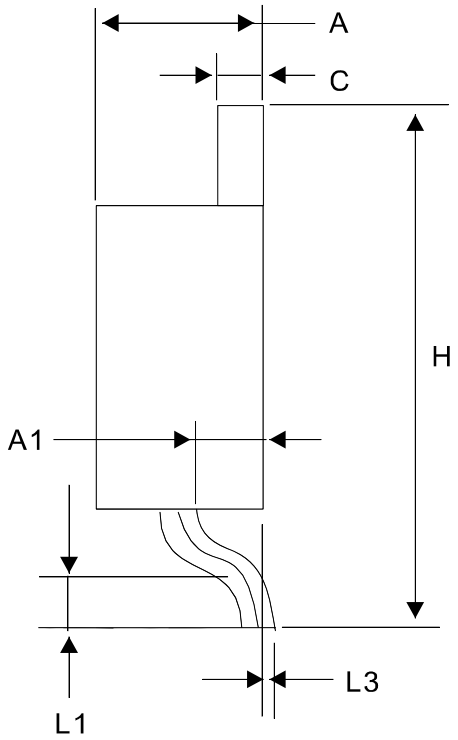
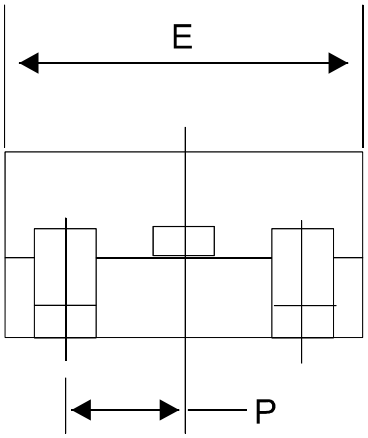
TO-252 Package Outline







SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.250	2.350	0.089	0.093
A1	0.950	1.050	0.037	0.041
C	0.490	0.530	0.019	0.021
E	6.400	6.600	0.252	0.260
E2	5.300	5.450	0.209	0.215
D	6.000	6.200	0.236	0.244
D2	7.100	7.300	0.280	0.287
H	9.700	10.100	0.382	0.398
L	0.600	Ref	0.024	Ref
L1	1.425	1.625	0.056	0.064
L2	0.650	0.850	0.026	0.033
L3	0.020	0.120	0.001	0.005
b	0.770	0.850	0.030	0.033
b1	0.840	0.940	0.033	0.037
P	2.290	BSC	0.090	BSC

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