N- and P-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4542 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 25m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leqq 40m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leqq 35m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leqq 58m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

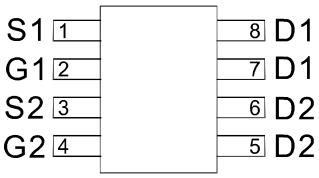
APPLICATIONS

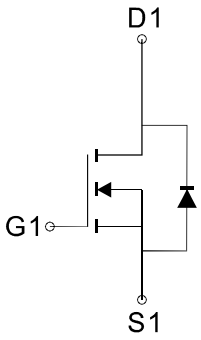
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION

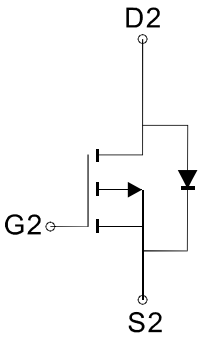
(SOP-8)

Top View





N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel		P-Channel		Unit
			10 secs	Steady State	10 secs	Steady State	
Drain-Source Voltage		V_{DSS}	30		-30		V
Gate-Source Voltage		V_{GSS}	±20		±20		V
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	8	6.3	-6.9	-5.4	A
	T_A=70℃		6.4	5	-5.5	-4.3	A
Pulsed Drain Current		I_{DM}	30		-30		A
Maximum Power Dissipation	T_A=25℃	P_D	2.6	1.6	2.7	1.6	W
	T_A=70℃		1.67	1	1.7	1	W
Operating Junction Temperature		T_J	-55 to 150				℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	48	78	46	77	℃/W
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	50		48		℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

N- and P-Channel 30-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
STATIC							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1.0 -1.0	1.5 -1.5	3.0 -3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V V_{DS}=-30V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
		V_{DS}=30V, V_{GS}=0V,T_J=55℃ V_{DS}=-30V, V_{GS}=0V,T_J=55℃	N-Ch P-Ch			25 -25	
$I_{D(ON)}$	On-State Drain Current[a]	V_{DS}≧5V, V_{GS}= 10V V_{DS}≦-5V, V_{GS}= -10V	N-Ch P-Ch	20 -20			A
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 6.7A V_{GS}=-10V, I_D= -6.1A	N-Ch P-Ch		21 30	25 35	mΩ
		V_{GS}=4.5V, I_D= 5.0A V_{GS}=-4.5V, I_D= -5.0A	N-Ch P-Ch		32 48	40 58	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=6.7A P-Channel V_{DS}=-15V, V_{GS}=-10V, I_D=-6.1A	N-Ch P-Ch		12 21	15 25	nC
Qgs	Gate-Source Charge		N-Ch P-Ch		2 4		
Qgd	Gate-Drain Charge		N-Ch P-Ch		2.5 6		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		360 840	420 980	pF
Coss	Output Capacitance		N-Ch P-Ch		70 120		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		17 32		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		0.5 5.5		Ω
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω P-Channel V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω	N-Ch P-Ch		9.3 32	13 41	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		14 13	18 17	
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32 58	41 75	
t_f	Turn-Off Fall Time		N-Ch P-Ch		3.2 6.8	5 9	

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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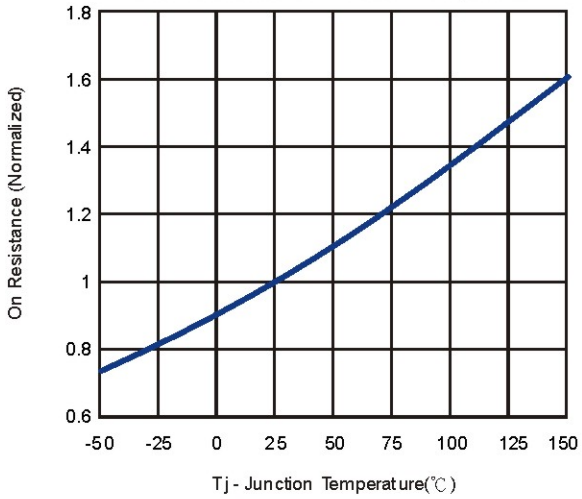
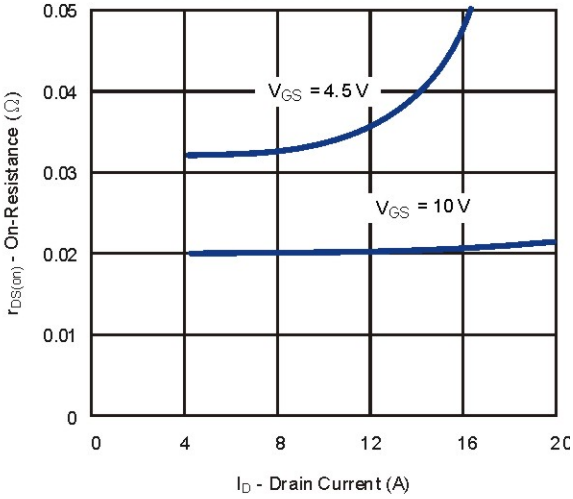
Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

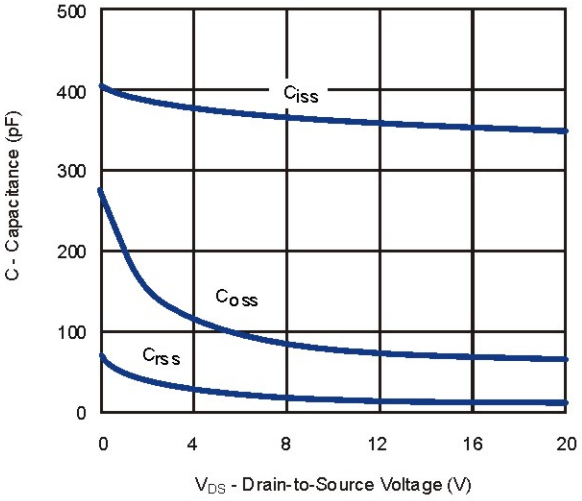
On Resistance vs. Junction Temperature



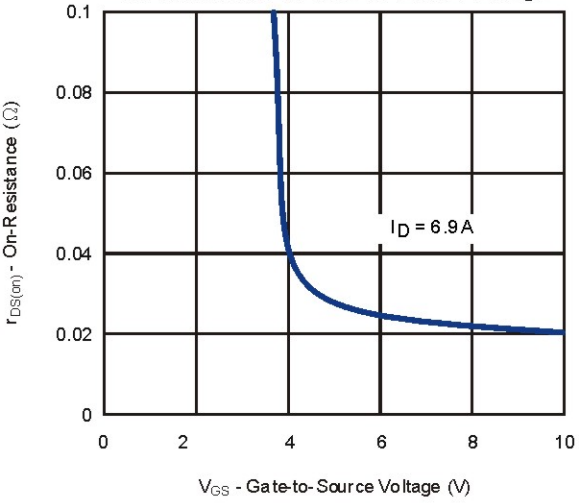
On-Resistance vs. Drain Current



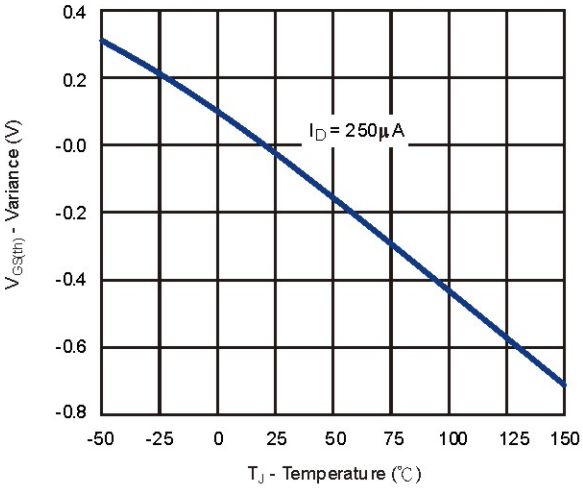
Capacitance



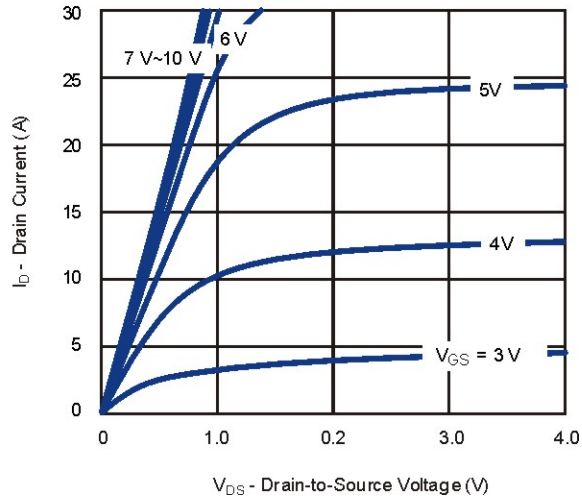
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



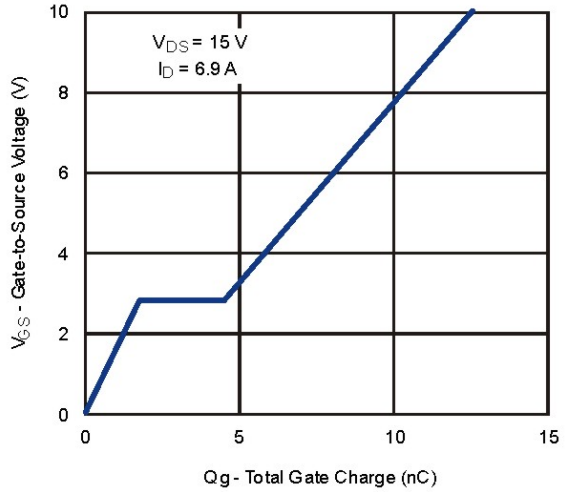
On-Region Characteristics



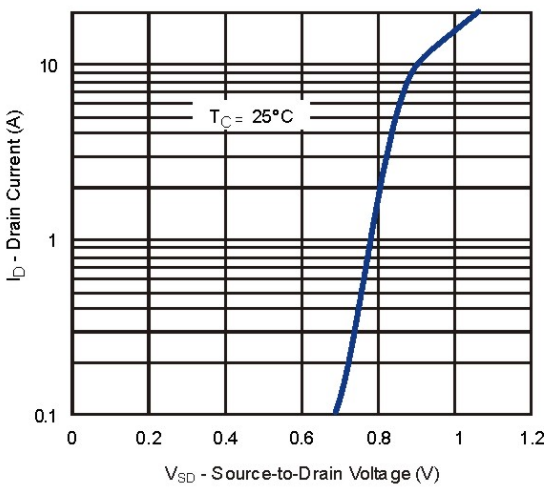
N- and P-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

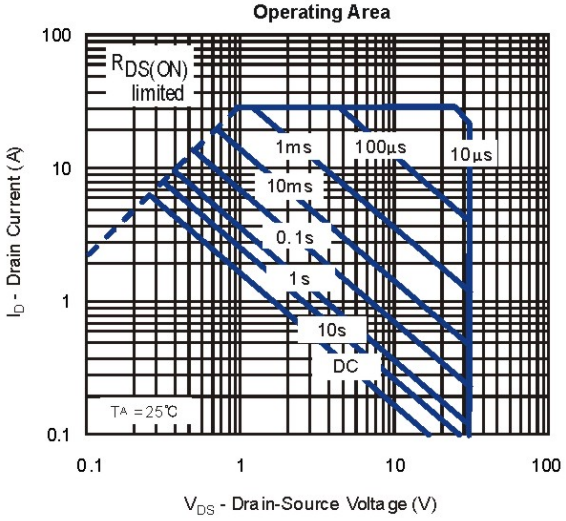
Gate Charge



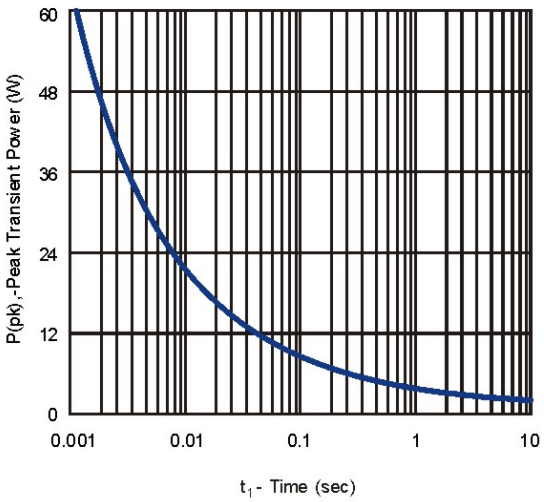
On-Resistance vs. Drain Current



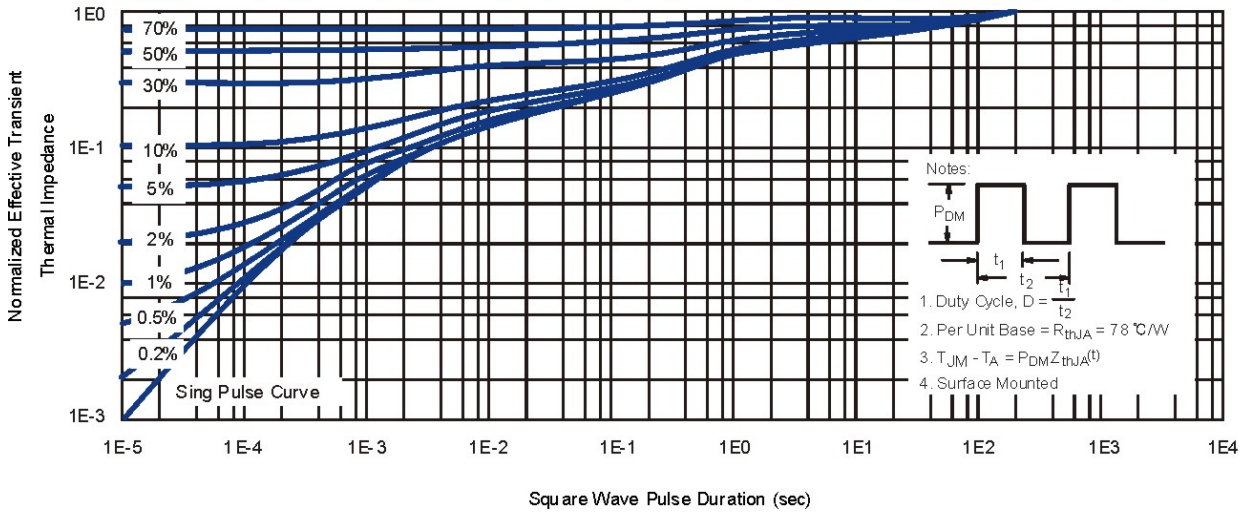
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation

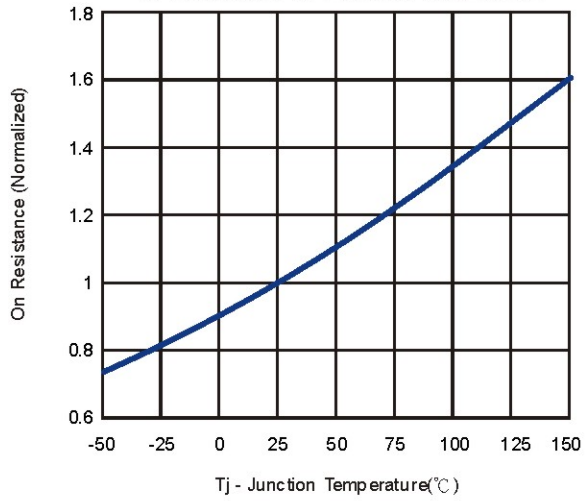


Normalized Thermal Transient Impedance, Junction-to-Ambient

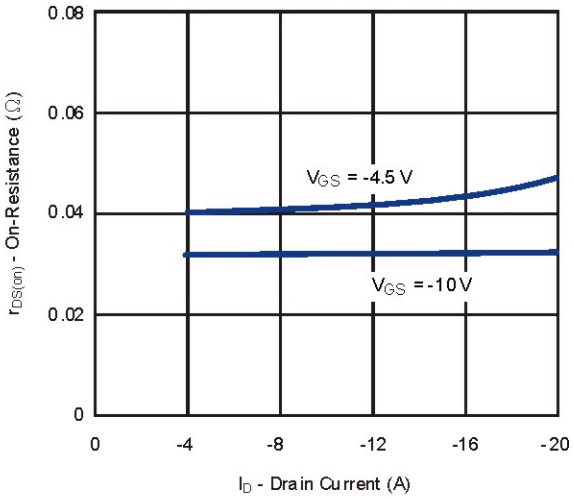


Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

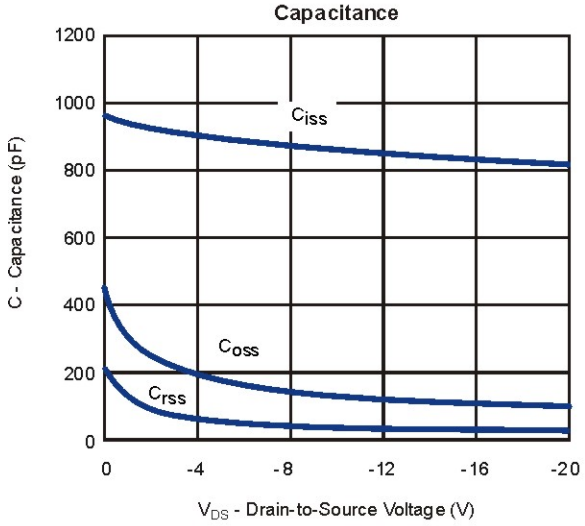
On Resistance vs. Junction Temperature



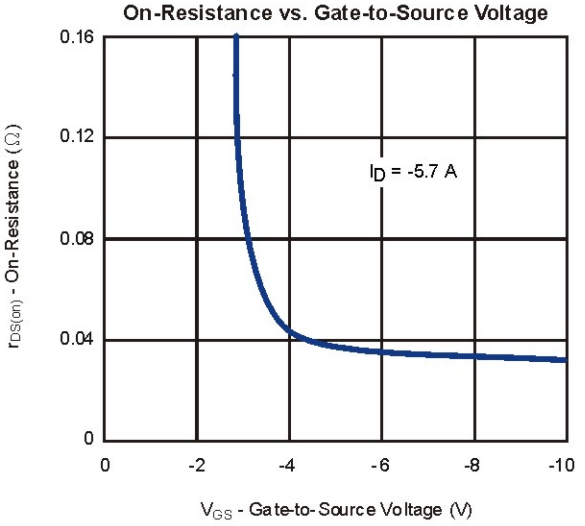
On-Resistance vs. Drain Current



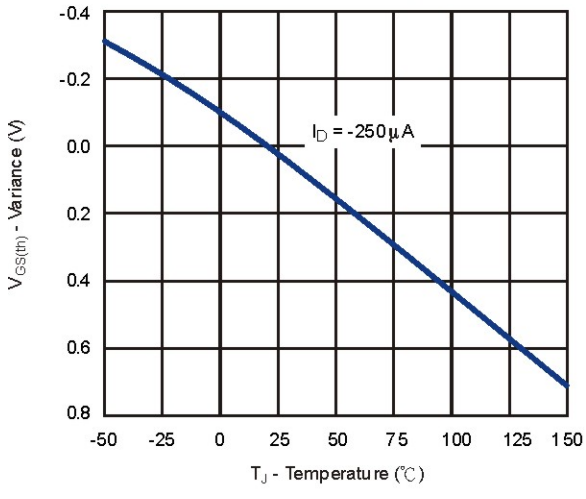
Capacitance



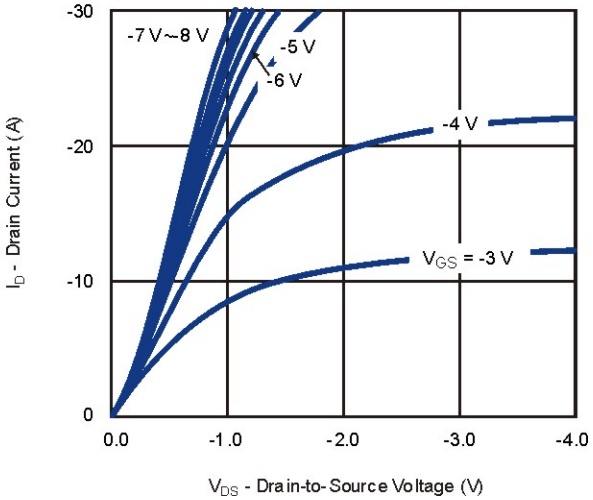
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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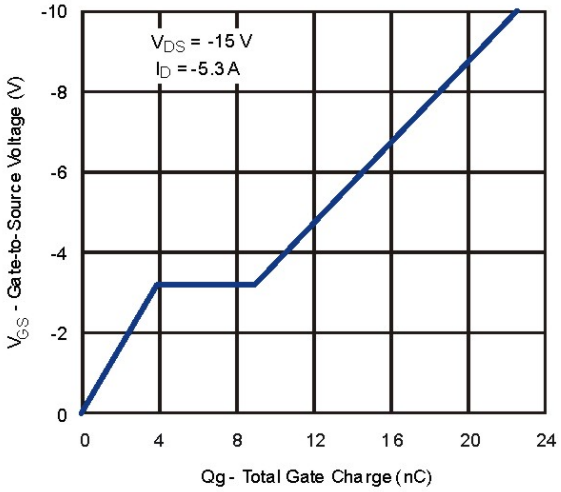
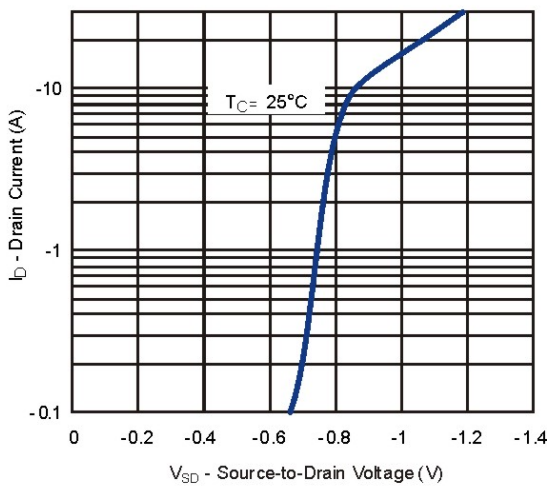
Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

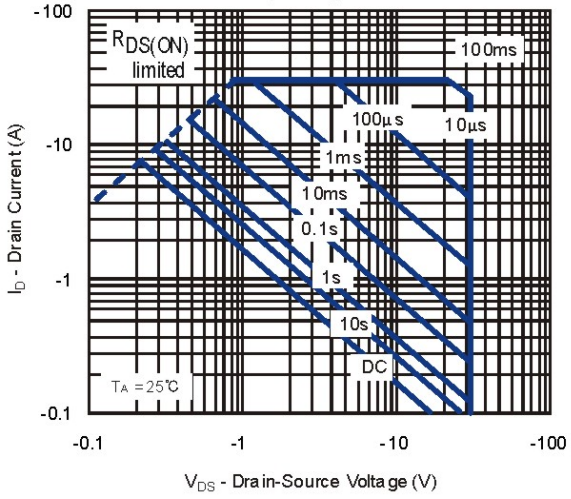
Gate Charge



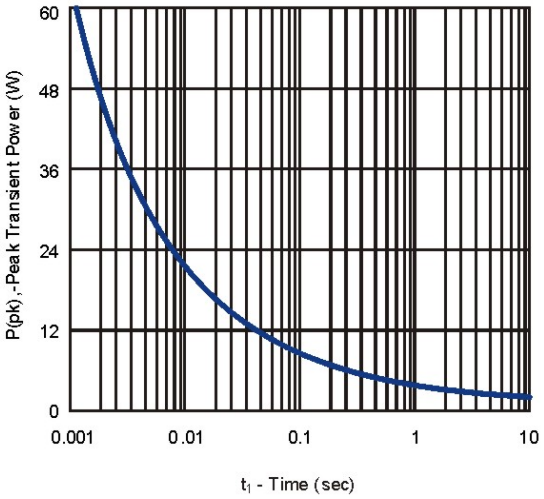
On-Resistance vs. Drain Current



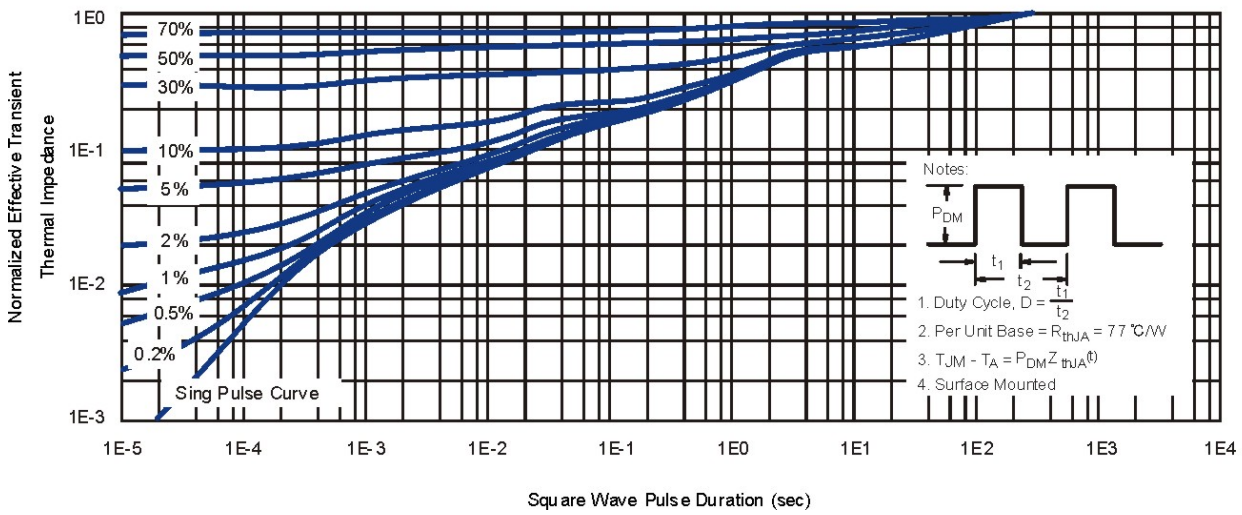
Maximum Forward Biased Safe Operating Area



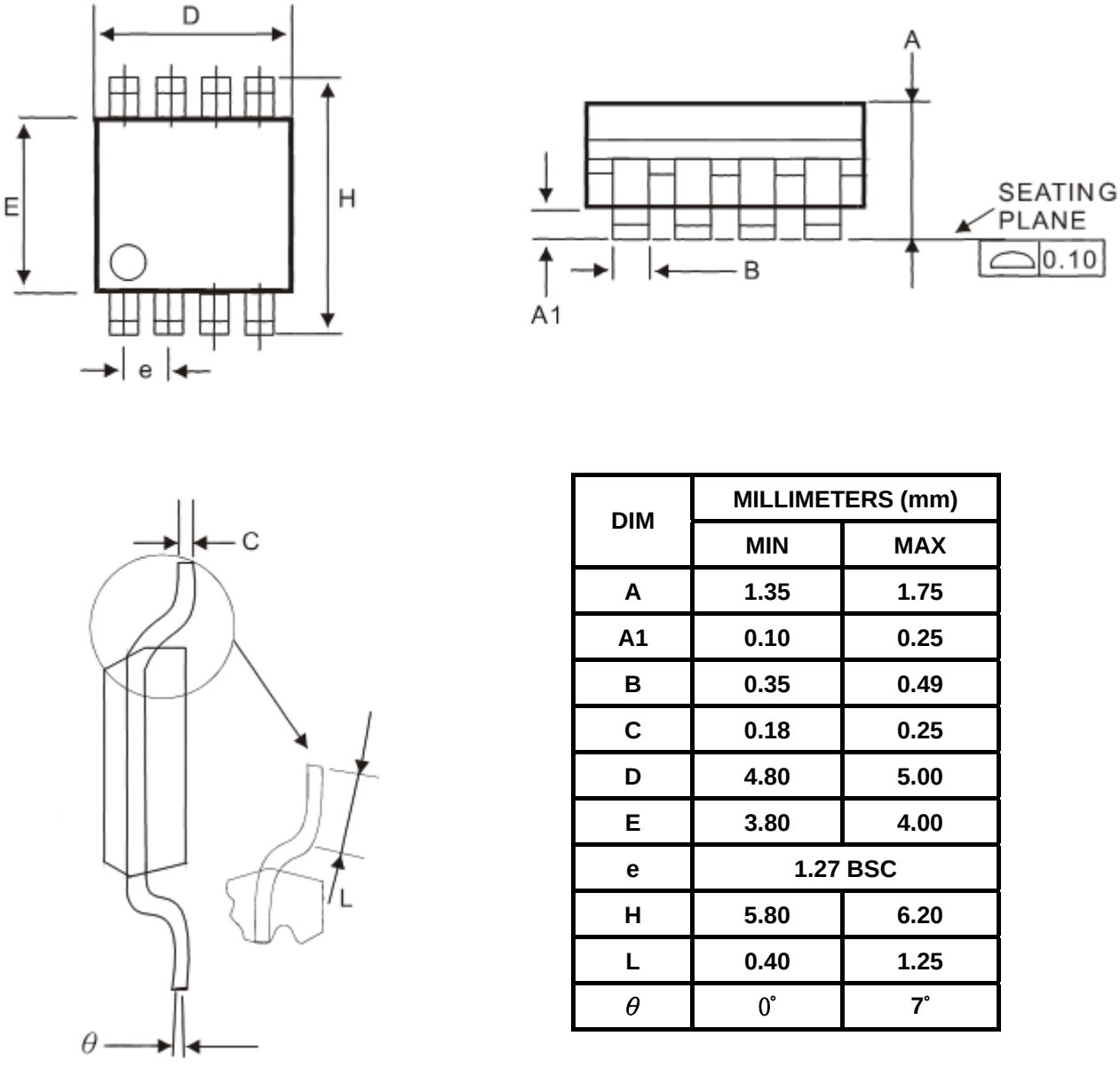
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.