N-Channel 60V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4436 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 33m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 40m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

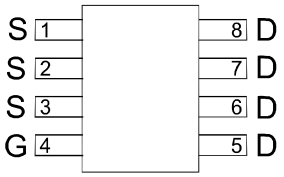
APPLICATIONS

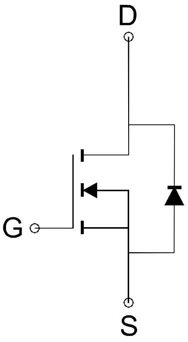
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET

Ordering Information: ME4436 (Pb-free)

ME4436-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	60		V
Gate-Source Voltage		V_{GSS}	±20		
Continuous Drain Current(Tj=150℃)	T_A=25℃	I_D	7.1	5.6	A
	T_A=70℃		5.7	4.5	
Pulsed Drain Current		I_{DM}	30		
Continuous Source-Drain Diode Current		I_S	2		
Avalanche Current	L=0.1mH	I_{AS}	15		
Single-Pulse Avalanche Energy		E_{AS}	12		mJ
Maximum Power Dissipation	T_A=25℃	P_D	2.7	1.6	W
	T_A=70℃		1.7	1	
Operating Junction & Storage Temperature Range		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	46	76	℃/W
Thermal Resistance-Junction to Case *		$R_{\theta JC}$	43		

*The device mounted on $1in^2$ FR4 board with 2 oz copper

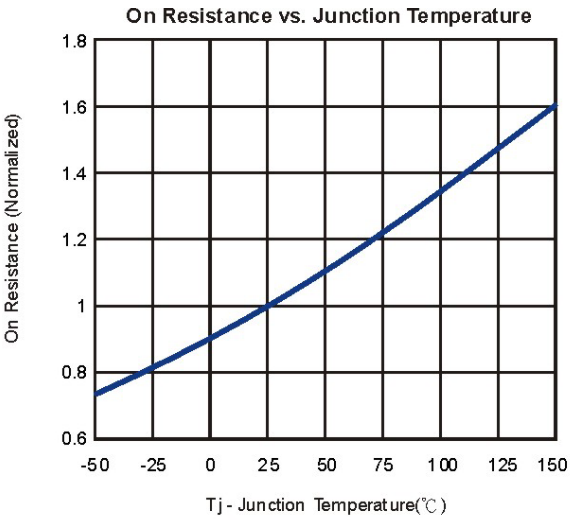
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

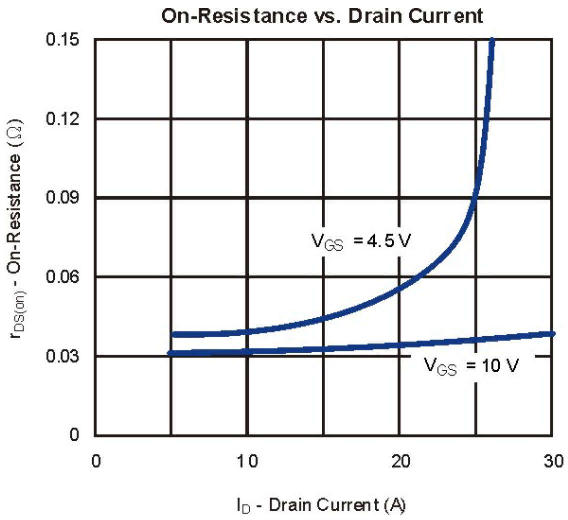
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
V_{DS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250µA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA	1.0	1.8	3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	µA
		V_{DS}=60V, V_{GS}=0V T_J=55℃			10	
$I_{D(ON)}$	On-State Drain Current[a]	V_{DS}≧5V, V_{GS}=10V	30			A
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 5.3A		26	33	mΩ
		V_{GS}=4.5V, I_D= 4.7A		31	40	
V_{SD}	Diode Forward Voltage	I_S=2A		0.8	1.2	V
DYNAMIC						
Ciss	Input capacitance	V_{DS}=30V, V_{GS}=0V, f=1.0MHz		940	1100	pF
Coss	Output Capacitance			71		
Crss	Reverse Transfer Capacitance			33		
Qg	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_D=5.3A		22	29	nC
		V_{DS}=30V, V_{GS}=5V, I_D=5.3A		13.3	18	
Qgs	Gate-Source Charge			7.1		
Qgd	Gate-Drain Charge			7.5		
Rg	Gate Resistance	f=1MHz		0.9		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L =6.8Ω I_D=4.4A, V_{GEN}=10V R_G=1Ω		14	18	ns
t_r	Turn-On Rise Time			26	33	
$t_{d(off)}$	Turn-Off Delay Time			41	52	
t_f	Turn-Off Fall Time			3.6	6	
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L =6.8Ω I_D=4.4A, V_{GEN}=4.5V R_G=1Ω		12	16	
t_r	Turn-On Rise Time			26	33	
$t_{d(off)}$	Turn-Off Delay Time			42	52	
t_f	Turn-Off Fall Time			3.8	7	

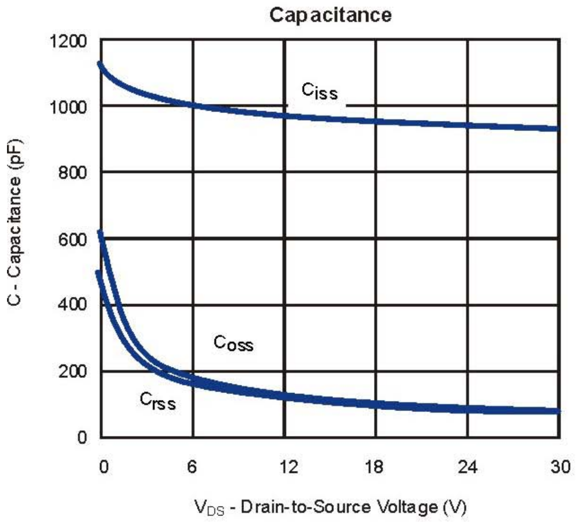
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

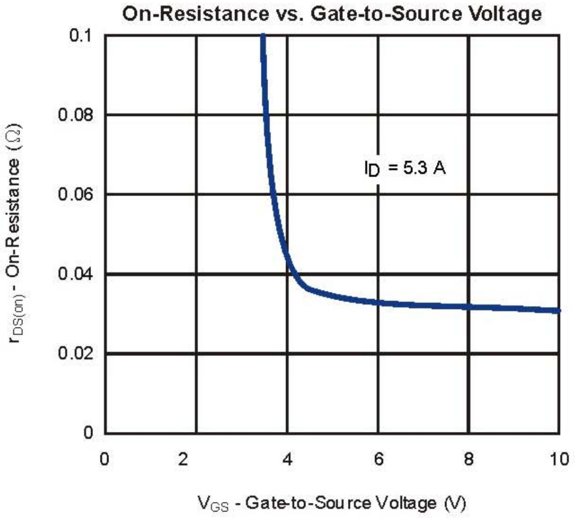
b. Matsuki reserves the right to improve product design, functions and reliability without notice.

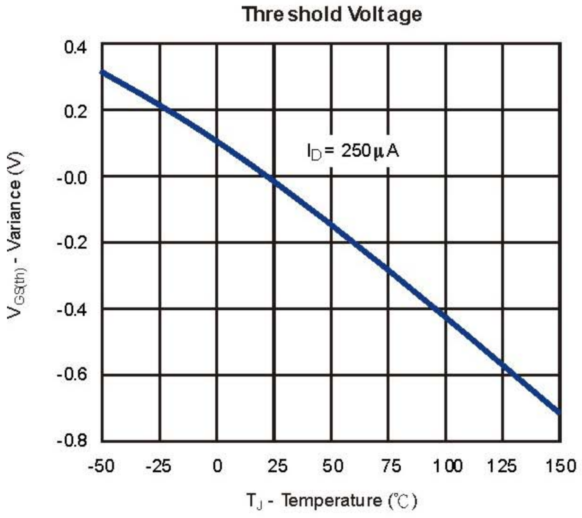
Typical Characteristics (TJ =25℃ Noted)

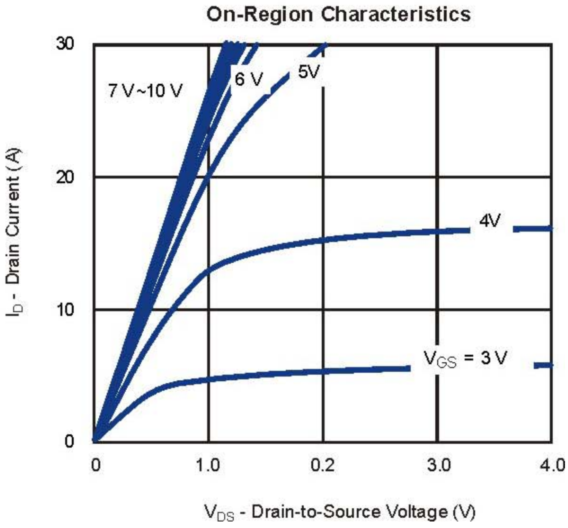




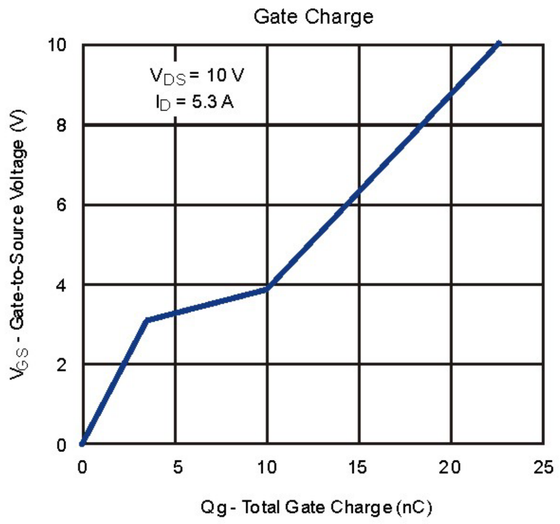




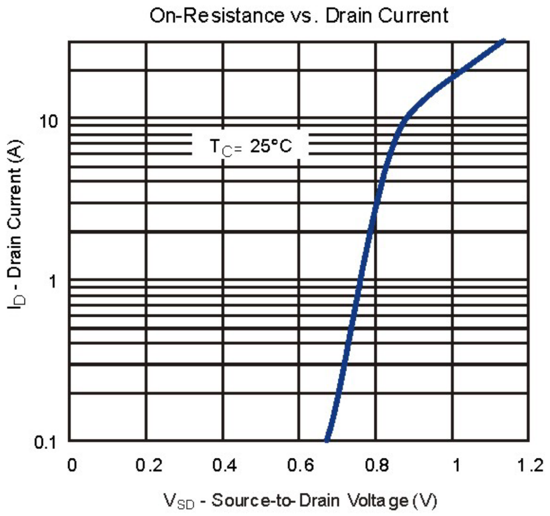




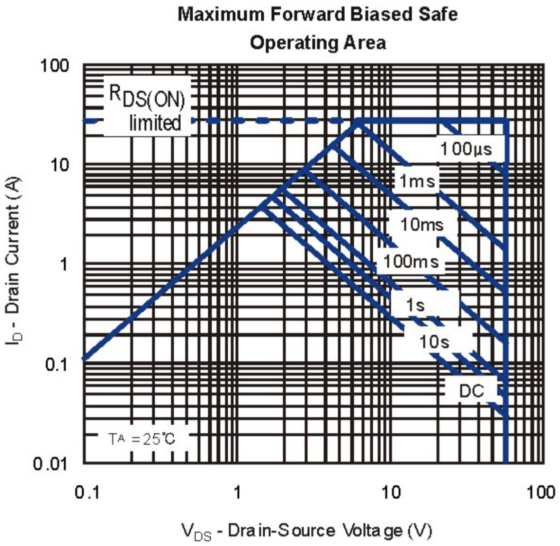
Typical Characteristics (T_J =25℃ Noted)



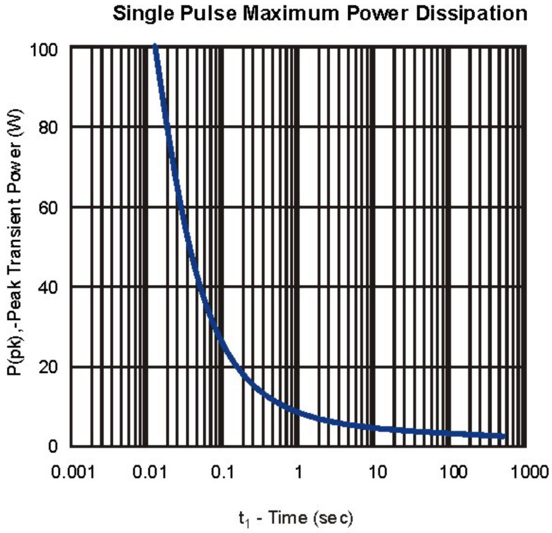
Gate Charge



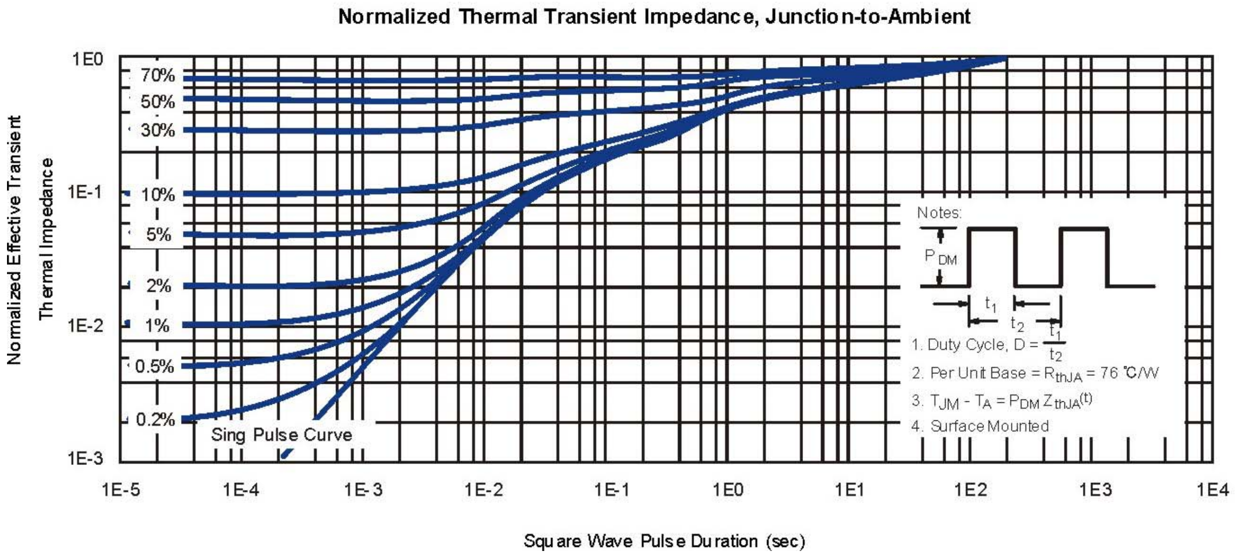
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation

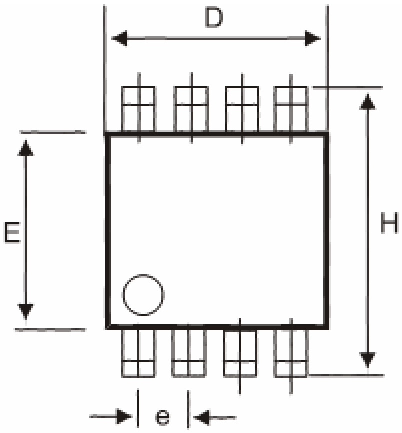


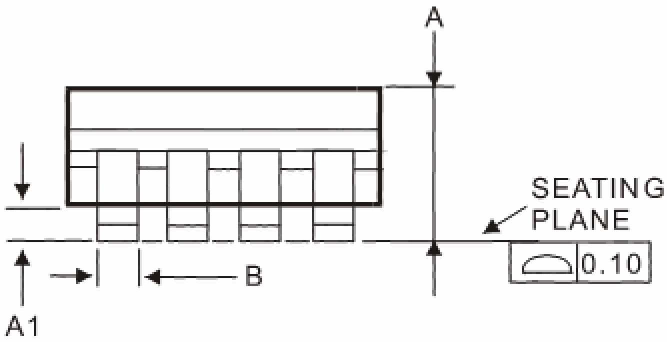
Normalized Thermal Transient Impedance, Junction-to-Ambient

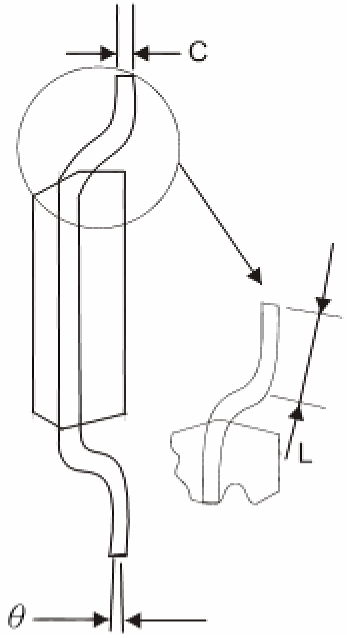
Notes:

1. Duty Cycle, $D = \frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 76 ℃/W
3. $T_{JM} - T_A = P_{DM} Z_{thJA}(t)$
4. Surface Mounted

SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.