N- and P-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4565AD4 is the N and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦30mΩ@V_{GS}=10V (N-Ch)
- $R_{DS(ON)}$ ≦58mΩ@V_{GS}=4.5V (N-Ch)
- $R_{DS(ON)}$ ≦45mΩ@V_{GS}=-10V (P-Ch)
- $R_{DS(ON)}$ ≦75mΩ@V_{GS}=-4.5V(P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

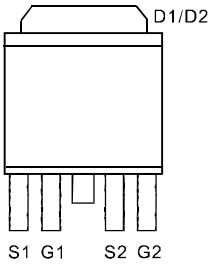
APPLICATIONS

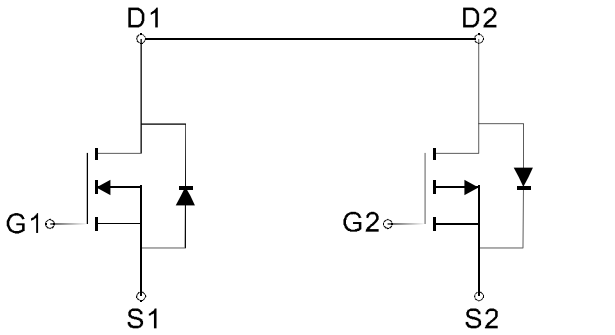
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-252-4L)

Top View





N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	±25	±25	V
Continuous Drain Current(Tj=150℃)*	T_C=25℃	I_D	22.1	-18.6	A
	T_C=70℃		17.7	-14.9	
	T_A=25℃		7.4	-6.1	
	T_A=70℃		5.9	-5	
Pulsed Drain Current		I_{DM}	30	-30	A
Maximum Power Dissipation	T_A=25℃	P_D	2.6	2.7	W
	T_A=70℃		1.67	1.7	
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Steady 48	Steady 46	℃/W
			10sec 20	10sec 18	
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	5.3	5	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N- and P-Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA V_{GS}=0V, I_D=250μA	N-Ch P-Ch	40 -40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1 -1		3 -3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V V_{DS}=0V, V_{GS}=±25V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V V_{DS}=-40V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
		V_{DS}=40V, V_{GS}=0V,T_J=55℃ V_{DS}=-40V, V_{GS}=0V,T_J=55℃	N-Ch P-Ch			10 -10	
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 7A V_{GS}=-10V, I_D= -7A	N-Ch P-Ch		23 36	30 45	mΩ
		V_{GS}=4.5V, I_D= 6A V_{GS}=-4.5V, I_D= -6A	N-Ch P-Ch		42 58	58 75	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.7 -0.7	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=20V, V_{GS}=4.5V, I_D=7A P-Channel V_{DS}=-20V, V_{GS}=-4.5V, I_D=-7A	N-Ch P-Ch		8 10		nC
Qgs	Gate-Source Charge		N-Ch P-Ch		4 4.3		
Qgd	Gate-Drain Charge		N-Ch P-Ch		4 4.5		
Rg	Gate Resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz V_{GS}=0V, V_{DS}=0V, f=1MHz	N-Ch P-Ch		0.7 6		Ω
Ciss	Input capacitance	N-Channel V_{DS}=20V, V_{GS}=0V, F=1MHz P-Channel V_{DS}=-20V, V_{GS}=0V, F=1MHz	N-Ch P-Ch		560 860		pF
Coss	Output Capacitance		N-Ch P-Ch		72 120		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		18 35		
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=15V, R_L=15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω P-Channel V_{DD}=-15V, R_L=15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω	N-Ch P-Ch		11 30		ns
t_r	Turn-On Rise Time		N-Ch P-Ch		13 8.5		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		37 70		
t_f	Turn-On Fall Time		N-Ch P-Ch		3.5 7		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

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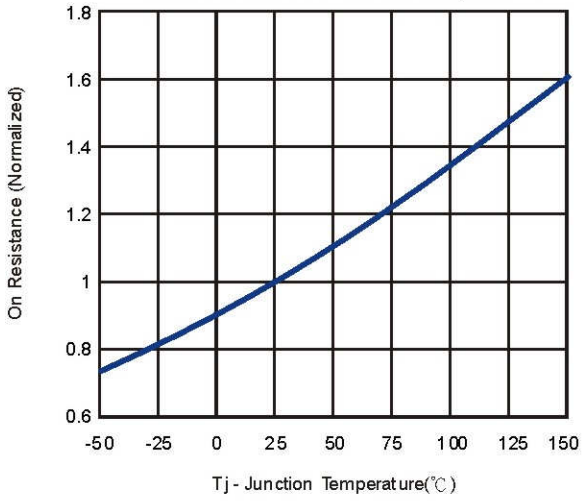
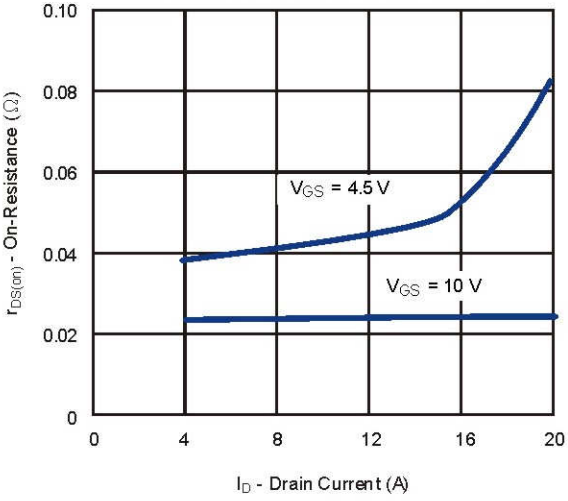
Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

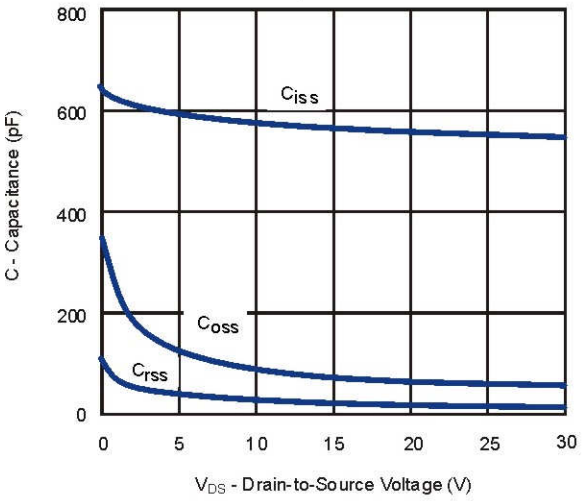
On Resistance vs. Junction Temperature



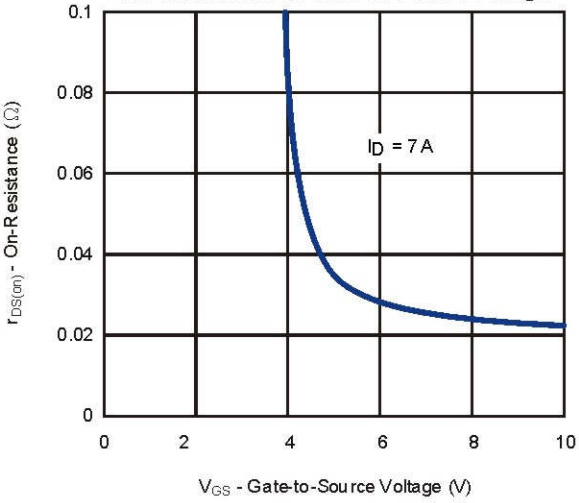
On-Resistance vs. Drain Current



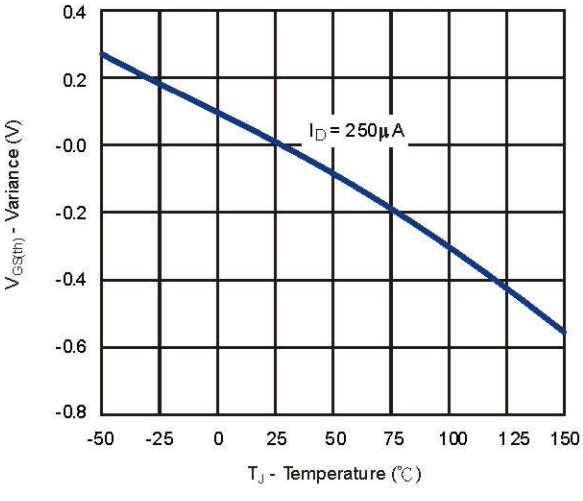
Capacitance



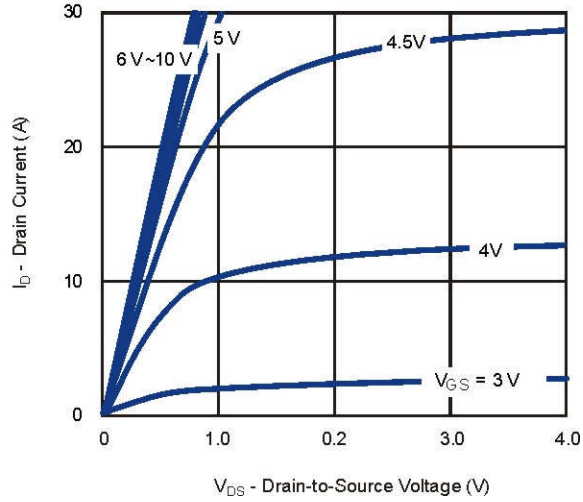
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



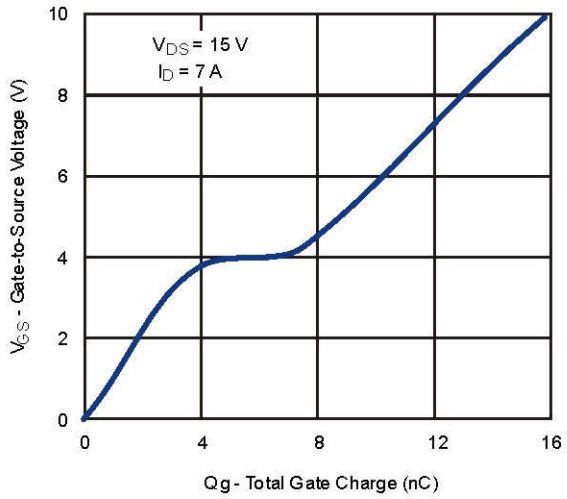
On-Region Characteristics



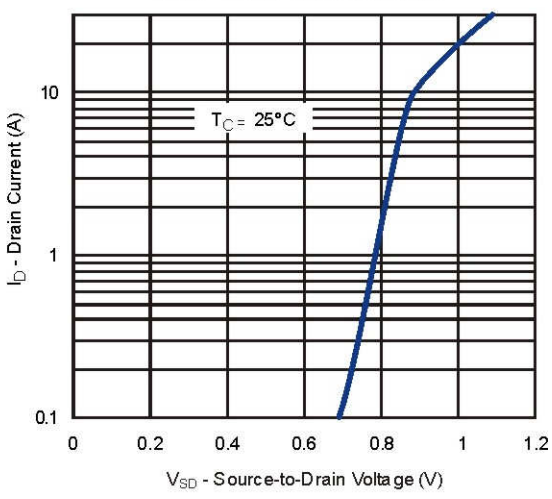
N- and P-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

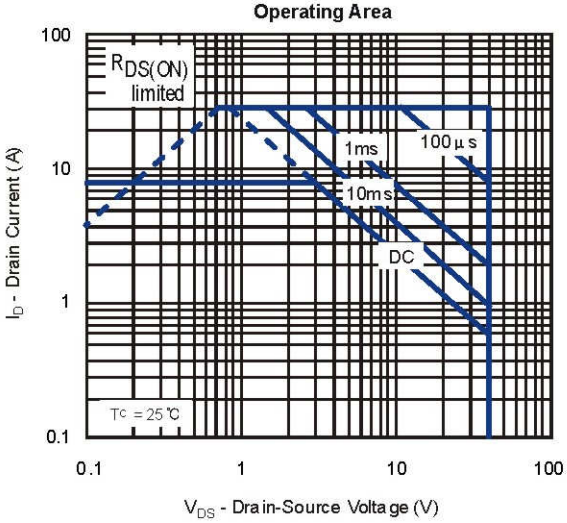
Gate Charge



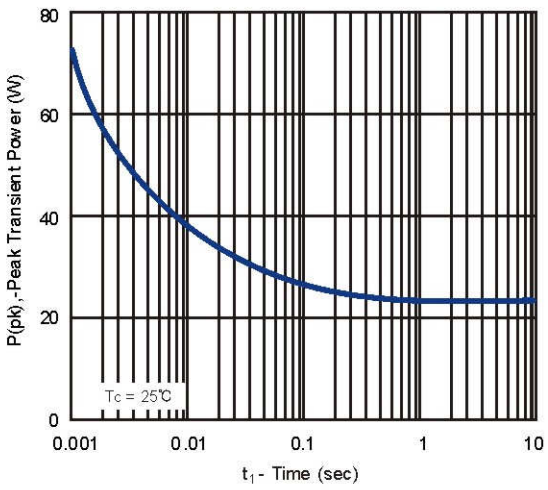
Body - Diode Characteristics



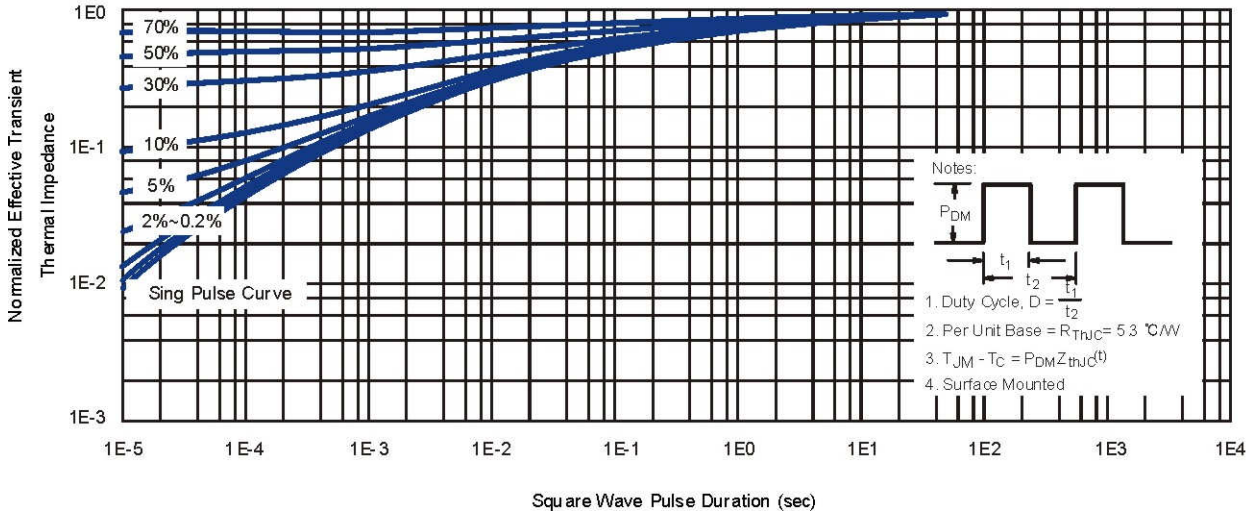
Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



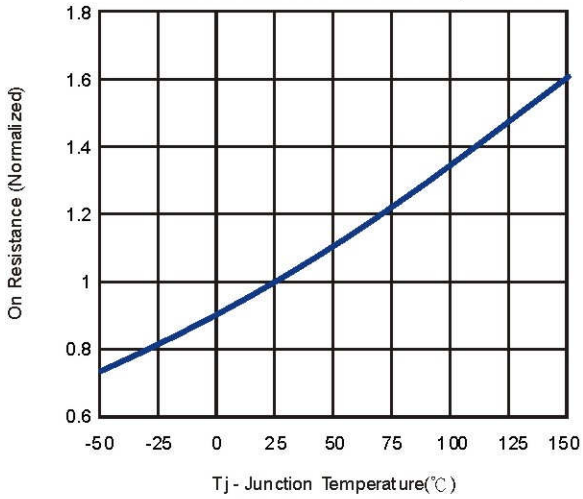
Normalized Thermal Transient Impedance, Junction-to-Case



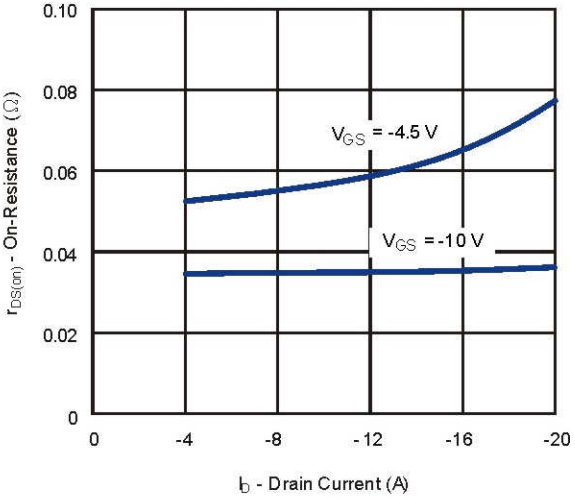
N- and P-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

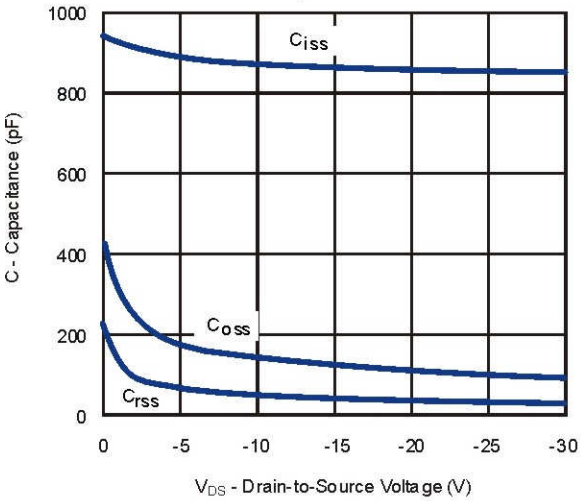
On Resistance vs. Junction Temperature



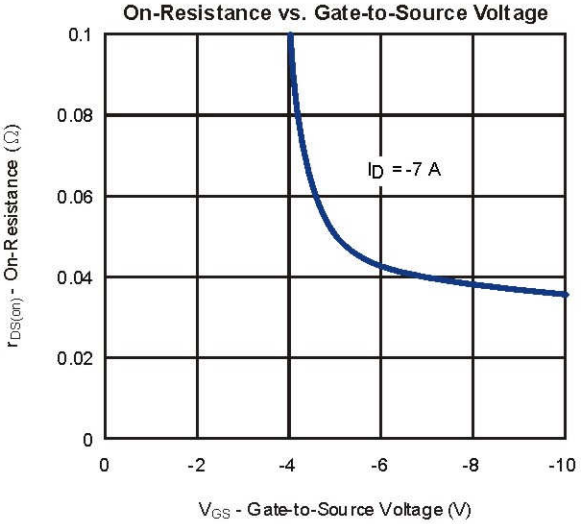
On-Resistance vs. Drain Current



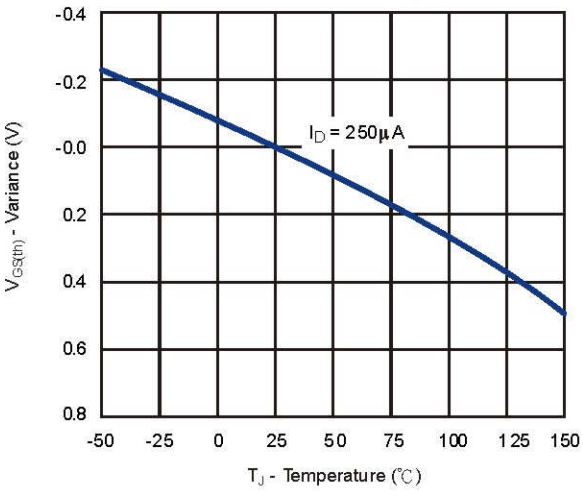
Capacitance



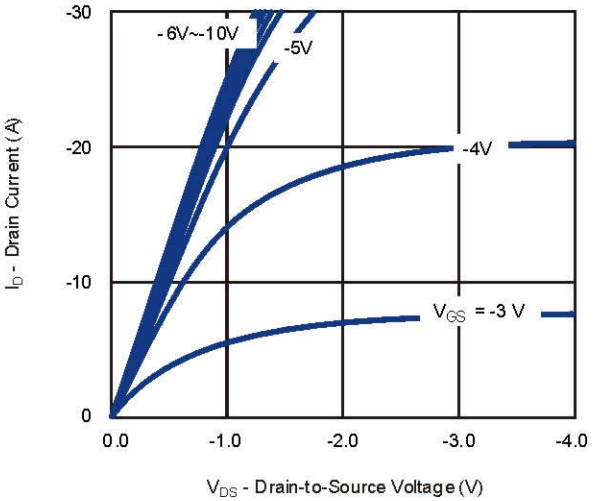
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



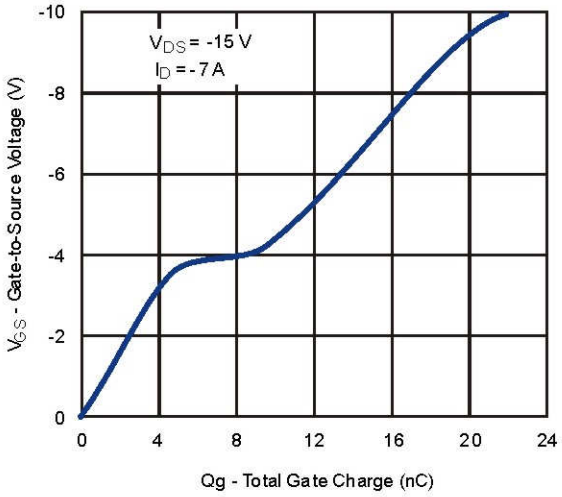
On-Region Characteristics



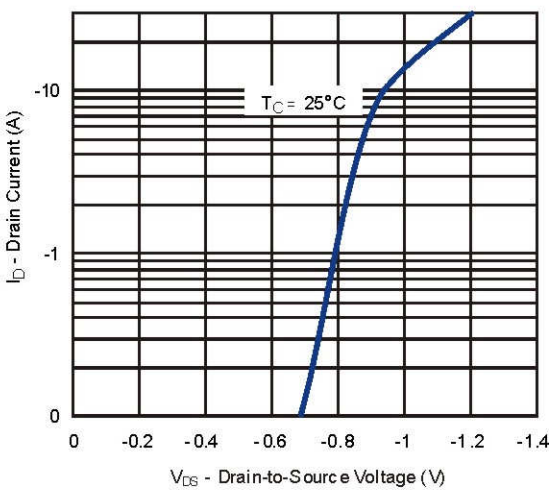
N- and P-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

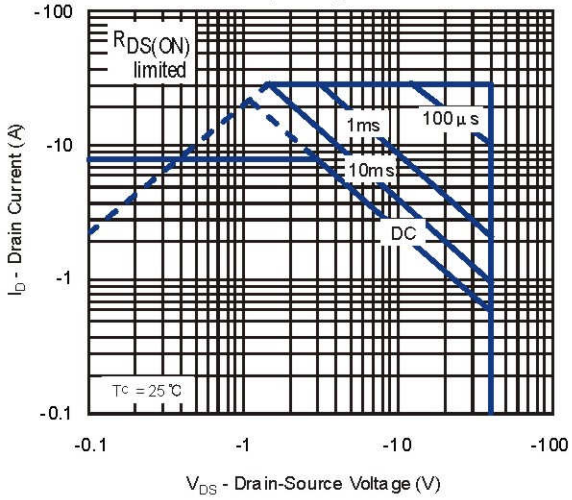
Gate Charge



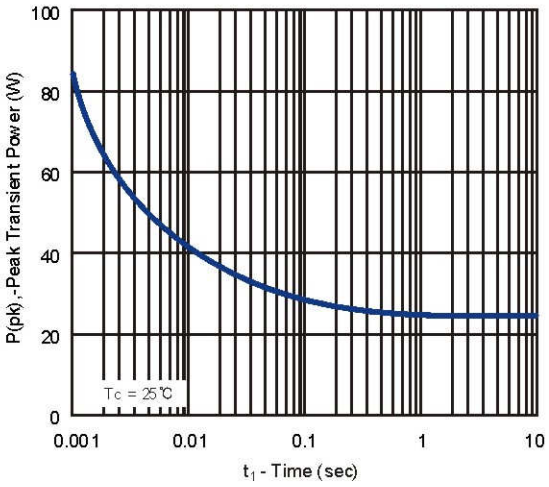
Body - Diode Characteristics



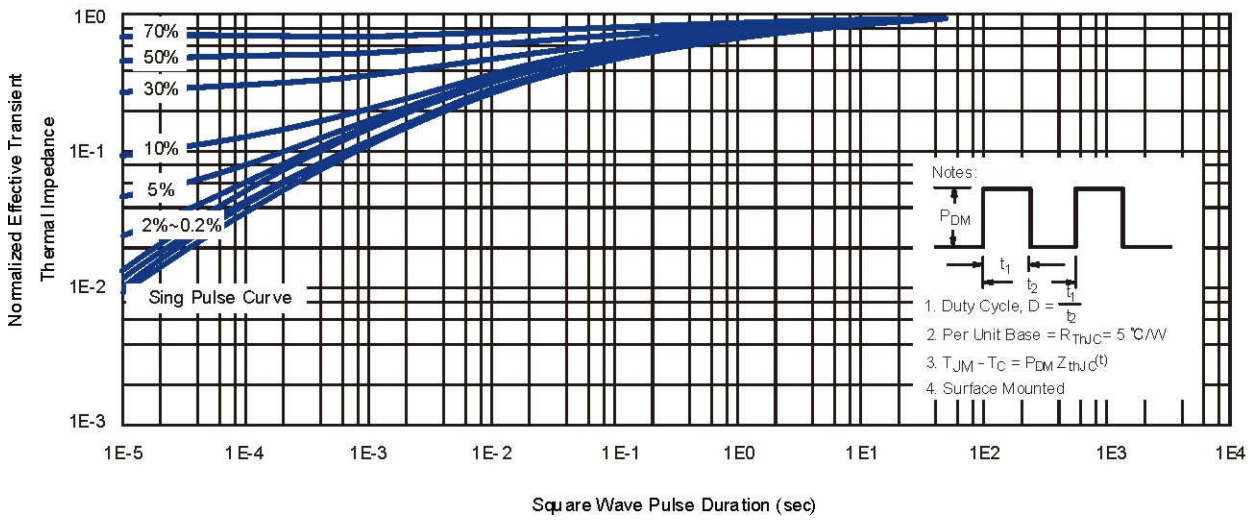
Maximum Forward Biased Safe Operating Area



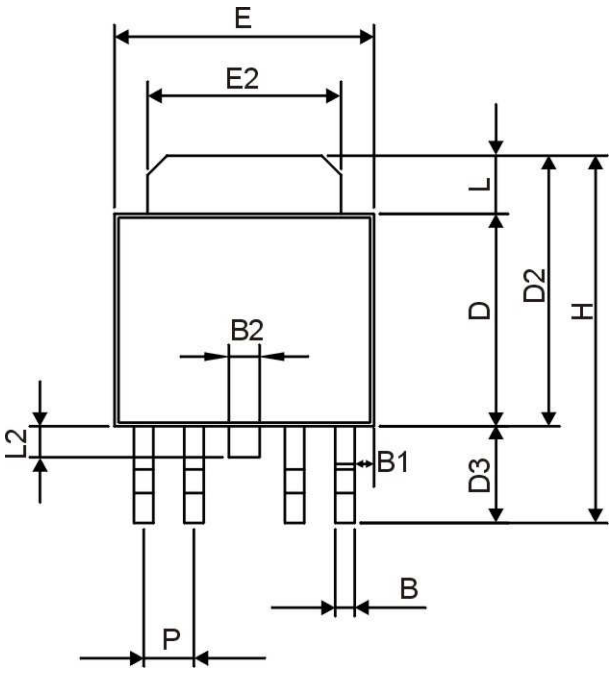
Single Pulse Maximum Power Dissipation

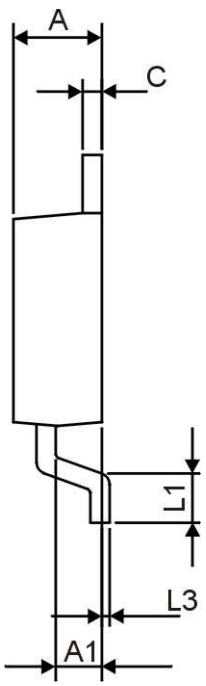


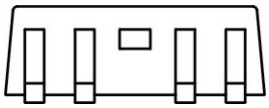
Normalized Thermal Transient Impedance, Junction-to-Case



TO-252-4L Package







DIM	MILLIMETERS	
	MIN	MAX
A	2.10	2.50
A1	1.10	1.30
B	0.30	0.70
B1	0.55	0.75
B2	0.40	0.80
C	0.40	0.60
D	5.30	5.70
D2	6.70	7.30
D3	2.20	3.00
E	6.30	6.70
E2	4.80	5.20
H	9.20	9.80
L	1.30	1.70
L1	0.90	1.50
L2	0.50	1.10
L3	0.00	0.30
P	1.20	1.40