

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - **5.0** Volts POWER DISSIPATION - **120** WATTS

GENERAL DESCRIPTION

The L12ESDL5V0C6-4 is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Protects up to four I/O lines (Data lines) & power line (Vcc pin5)
- Low capacitance: 0.3pF typical (I/O to I/O)
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air); > ±8KV (contact).

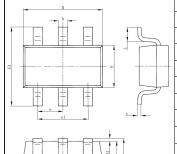
APPLICATION

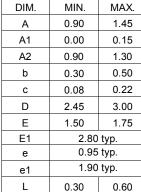
- High Definition Multimedia Interface (HDMI)
- Digital Visual Interface (DVI)
- Monitors and Flat Panel Displays
- USB 2.0
- USB OTG
- IEEE 1394 Firewire Port

MECHANICAL DATA

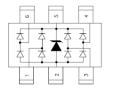
- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2002/95/E

<u>SOT23-6L</u>





SOT23-6L



Ground

All Dimensions in millimeter

4 lines Protection

MAXIMUM RATINGS (Tj= 25[°]C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	Ppk	120	W
Peak Pulse Current (tp = 8/20us)	Ipp	5	Α
Operating Junction Temperature Range	TJ	-55 to + 125	$^{\circ}\mathbb{C}$
Storage Temperature Range	Tstg	-55 to + 150	$^{\circ}$ C
Soldering Temperature, t max = 10s	TL	260	$^{\circ}\mathbb{C}$

ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	MIn	Тур	Max	Unit
Reverse standoff voltage	V_{RWM}	Any pin to ground			5.0	V
Breakdown voltage	VBR	IR = 1 mA	6.0			V
Reverse leakage current	IRM	V _{DRM} = 5V			1	uA
Clamping Voltage	Vc	I_{PP} = 1A, tp = 8/20 μ s, Any I /O pin to ground			15	V
Clamping Voltage	Vc	I_{PP} = 5A, tp = 8/20µs, Any I/O pin to ground			24	V
Junction capacitance	CJ	V_R = 2.5V, f = 1MHz, Any I/O pin to ground			0.8	pF
Junction capacitance	C _J	V _R = 2.5V, f = 1MHz, Between I/O pins			0.4	pF
	•			REV. 3.	Jan-2013	KSIR53



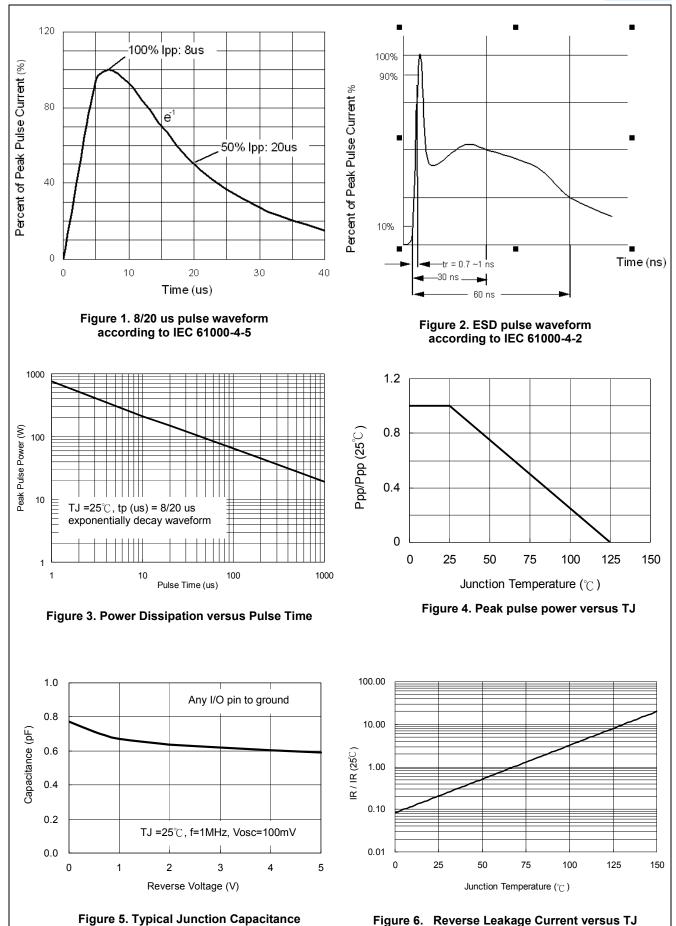


Figure 6. Reverse Leakage Current versus TJ



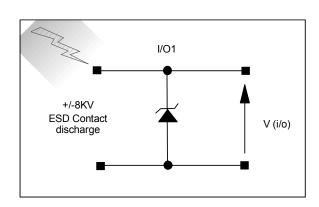


Figure 7. ESD Test Configuration

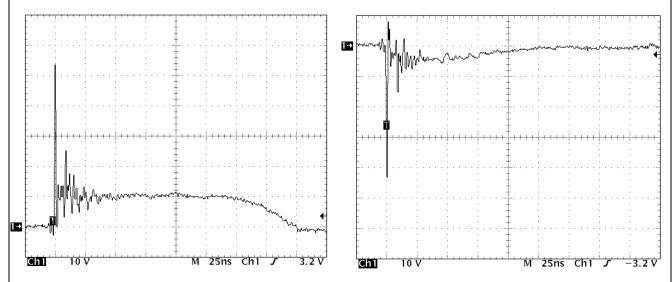
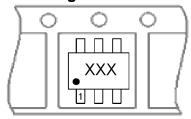


Figure 8. Clamped +8 kV ESD voltage waveform

Figure 9. Clamped -8 kV ESD voltage waveform



Marking & Orientation

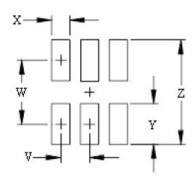


DEVICE	Wire	Marking	Packing
L12ESDL5V0C6-4	Au	LC5	Taping / Reel
L12ESDL5V0C6-4C	Cu	LCV	Taping / Reel

Packaging Information

DEVICE	Q'TY/REEL	REEL DIA.	Q'TY/BOX	Q'TY/CARTON
	(PCS)	(INCH)	(PCS)	(PCS)
L12ESDL5V0C6-4 L12ESDL5V0C6-4C	3000	7	45000	90K/180K

SOT23-6L Soldering Pad Layout



Dim.	Millimeters	Inches
Z	3.60	0.141
X	0.80	0.031
W	2.60	0.102
Y	1.00	0.039
V	0.95	0.037

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