NL17SZ74

Single D Flip Flop

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

Features

- Extremely High Speed: t_{PD} 2.6 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 5.0 V Tolerant Inputs − Interface Capability with 5.0 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Replacement for NC7SZ74
- Tiny Ultra Small Package Only 2.1 X 3.0 mm
- High ESD Ratings: 4000 V Human Body Model
  200 V Machine Model
- Chip Complexity: FET = 64
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

TRUTH TABLE

Inputs				Outputs		
$\overline{PR}$	$\overline{CLR}$	CP	D	Q	$\overline{Q}$	Operating Mode
L H L	H L L	X X X	X X X	H L H	L H H	Asynchronous Set Asynchronous Clear Undetermined
H H	H H	↑ ↑	h l	H L	L H	Load and Read Register
H	H	↥	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low−to−High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low−to−High Transition
↥ = Not a Low−to−High Transition
For I_{CC} reasons, DO NOT FLOAT Inputs

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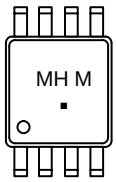
US8
US SUFFIX
CASE 493

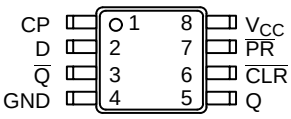
MARKING DIAGRAM



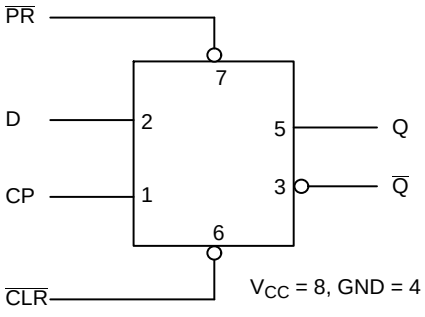
MH = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUT DIAGRAM



LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{CC}	DC Supply Voltage	−0.5 to +7.0	V
V_I	DC Input Voltage	−0.5 to +7.0	V
V_O	DC Output Voltage − Output in High or Low State (Note 1)	−0.5 to V_{CC} +0.5	V
I_{IK}	DC Input Diode Current V_I < GND	−50	mA
I_{OK}	DC Output Diode Current V_O < GND	−50	mA
I_O	DC Output Sink Current	±50	mA
I_{CC}	DC Supply Current Per Supply Pin	±100	mA
I_{GND}	DC Ground Current Per Ground Pin	±100	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	250	°C/W
P_D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F_R	Flammability Rating, Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	 >4000 >200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 6)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm X 1 inch, 2 ounce copper trace with no air flow.
3. Tested to EIA/JESD22−A114−A.
4. Tested to EIA/JESD22−A115−A.
5. Tested to JESD22−C101−A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	 1.65 1.5	 5.5 5.5	V
V_I	Input Voltage (Note 7)	0	5.5	V
V_O	Output Voltage (HIGH or LOW State)	0	5.5	V
T_A	Operating Free−Air Temperature	−55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate V_{CC} = 2.5 V ±0.2 V V_{CC} = 3.0 V ±0.3 V V_{CC} = 5.0 V ±0.5 V	 0 0 0	 20 10 5.0	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

ORDERING INFORMATION

Device	Package	Shipping†
NL17SZ74USG	US8 (Pb−Free)	3000 / Tape & Reel
NLV17SZ74USG*	US8 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25°C			−55°C ≤ T_A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65	0.75 V_{CC}			0.75 V_{CC}		V
			2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65			0.25 V_{CC}		0.25 V_{CC}	V
			2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}	
V_{OH}	High−Level Output Voltage V_{IN} = V_{IL} or V_{IL}	I_{OH} = 100 μA I_{OH} = −3 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V_{CC} 1.52 2.1 2.4 2.7 2.5 4.0		V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V_{OL}	Low−Level Output Voltage V_{IN} = V_{IH}	I_{OL} = 100 μA I_{OL} = 3 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.008 0.10 0.12 0.15 0.19 0.30 0.30	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0			1.0		10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V or GND	5.5			1.0		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

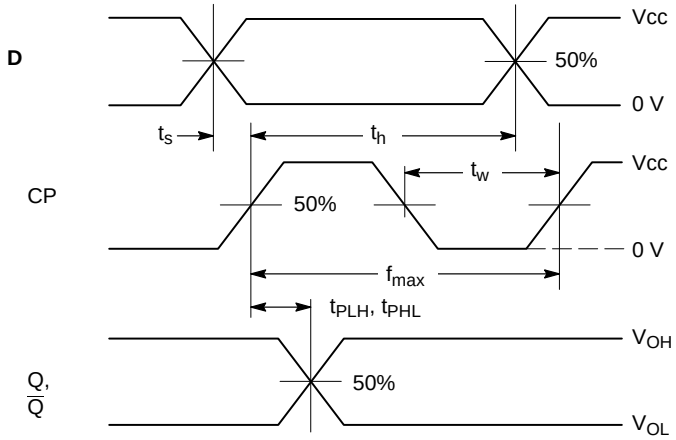
Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = 25°C			T_A = −55 to 125°C		Units
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	75			75		MHz
		2.5 ± 0.2		150			150		
		3.3 ± 0.3		200			200		
		5.0 ± 0.5		250			250		
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	175			175		
		5.0 ± 0.5		200			200		
t_{PLH}, t_{PHL}	Propagation Delay, CP to Q or $\overline{Q}$ (Waveform 1)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	2.5	6.5	12.5	2.5	13	ns
		2.5 ± 0.2		1.5	3.8	7.5	1.5	8.0	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	4.5	0.8	5.0	
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$ (Waveform 2)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	2.5	6.5	14	2.5	14.5	ns
		2.5 ± 0.2		1.5	3.8	9.0	1.5	9.5	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	5.0	0.8	5.5	
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t_S	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	6.5			6.5		ns
		2.5 ± 0.2		3.5			3.5		
		3.3 ± 0.3		2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
t_H	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	0.5			0.5		ns
		2.5 ± 0.2		0.5			0.5		
		3.3 ± 0.3		0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
t_W	Pulse Width, CP, $\overline{CLR}$, $\overline{PR}$ (Waveform 3)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	6.0			6.0		ns
		2.5 ± 0.2		4.0			4.0		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
t_{REC}	Recover Time $\overline{PR}$; $\overline{CLR}$ to CP (Waveform 3)	1.8 ± 0.15	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	8.0			8.0		ns
		2.5 ± 0.2		4.5			4.5		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		3.0			3.0		
		3.3 ± 0.3	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	3.0			3.0		
		5.0 ± 0.5		3.0			3.0		

8. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

CAPACITANCE (Note 9)

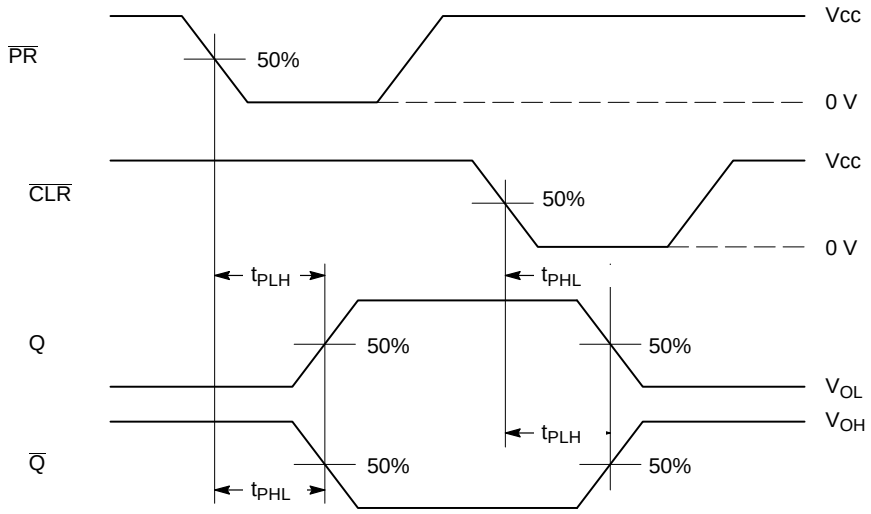
Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5 V	7.0	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V	7.0	pF
C_{PD}	Power Dissipation Capacitance (Note 10) Frequency = 10 MHz	V_{CC} = 3.3 V V_{CC} = 5.0 V	16 21	pF

9. T_A = +25°C, f = 1 MHz
10. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 1) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC(static)}$.



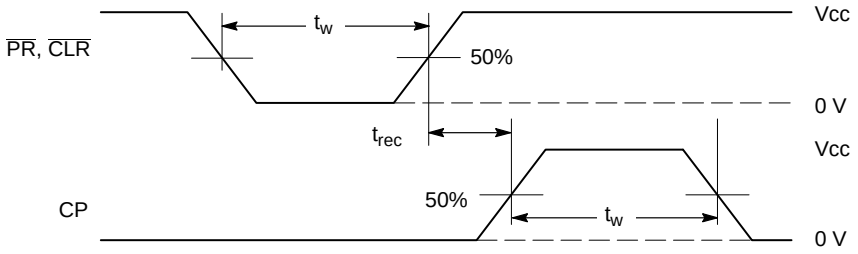
WAVEFORM 1 − PROPAGATION DELAYS, SETUP AND HOLD TIMES

$t_R = t_F$ = 3.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 − PROPAGATION DELAYS

$t_R = t_F$ = 3.0 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 − RECOVERY TIME

$t_R = t_F$ = 3.0 ns from 10% to 90%; f = 1 MHz; t_W = 500 ns

Output Reg: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

Figure 1. AC Waveforms

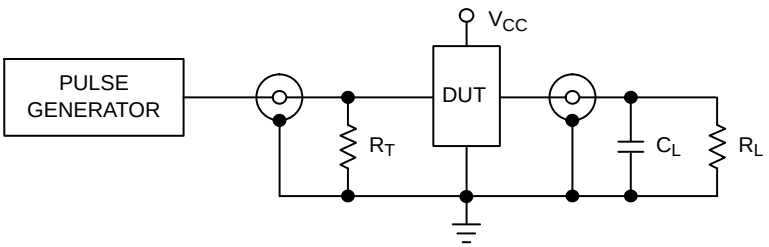
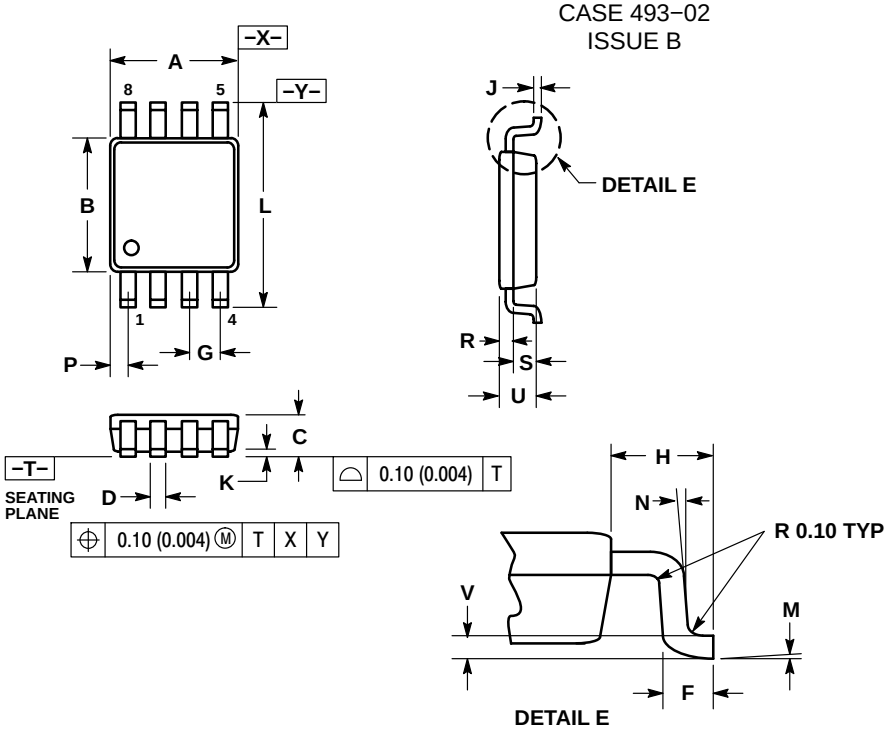


Figure 2. Test Circuit

PACKAGE DIMENSIONS

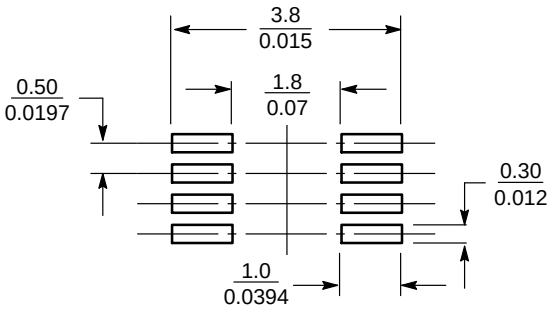
US8
US SUFFIX
CASE 493−02
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION “A” DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH. PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055”) PER SIDE.
4. DIMENSION “B” DOES NOT INCLUDE INTER−LEAD FLASH OR PROTRUSION. INTER−LEAD FLASH AND PROTRUSION SHALL NOT E3XCEED 0.140 (0.0055”) PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076−0.0203 MM. (300−800 “).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002 “).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0 °	6 °	0 °	6 °
N	5 °	10 °	5 °	10 °
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



SCALE 8:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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