ME80N75T / ME80N75T-G

N- Channel 75-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME80N75T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leqq 10m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

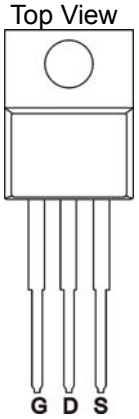
APPLICATIONS

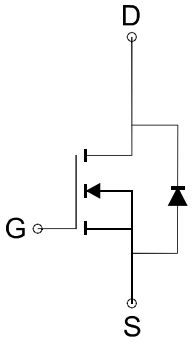
- Power Management
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-220)

Top View





N-Channel MOSFET

Ordering Information: ME80N75T (Pb-free)

ME80N75T-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	75	V
Gate-Source Voltage		V_{GSS}	±25	V
Continuous Drain Current*	T_C=25℃	I_D	93	A
	T_C=70℃		78	
Pulsed Drain Current		I_{DM}	372	A
Maximum Power Dissipation	T_C=25℃	P_D	200	W
	T_C=70℃		140	
Operating Junction and Storage Temperature Range		T_J	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.75	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	75			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=75V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=40A		8	10	mΩ
V_{SD}	Diode Forward Voltage *	I_S=40A, V_{GS}=0V		0.9	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=60V, V_{GS}=10V, I_D=75A		134		nC
Qg	Total Gate Charge	V_{DD}=60V, V_{GS}=4.5V, I_D=75A		27		
Qgs	Gate-Source Charge			36		
Qgd	Gate-Drain Charge			50		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.8		Ω
Ciss	Input Capacitance	V_{DS}=20V, V_{GS}=0V, f=1MHz		6200		pF
Coss	Output Capacitance			437		
Crss	Reverse Transfer Capacitance			144		
$t_{d(on)}$	Turn-On Delay Time	V_{GS} =10V, R_L=15Ω V_{DD}=30V, R_G=10Ω		60		ns
t_r	Turn-On Rise Time			43		
$t_{d(off)}$	Turn-Off Delay Time			159		
t_f	Turn-Off Fall Time			47		

Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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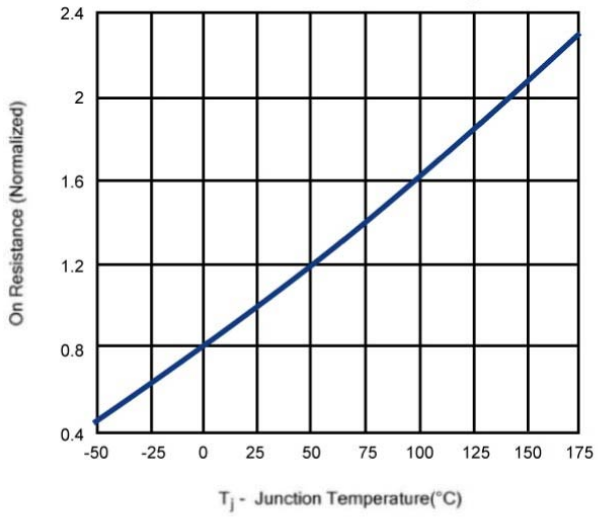
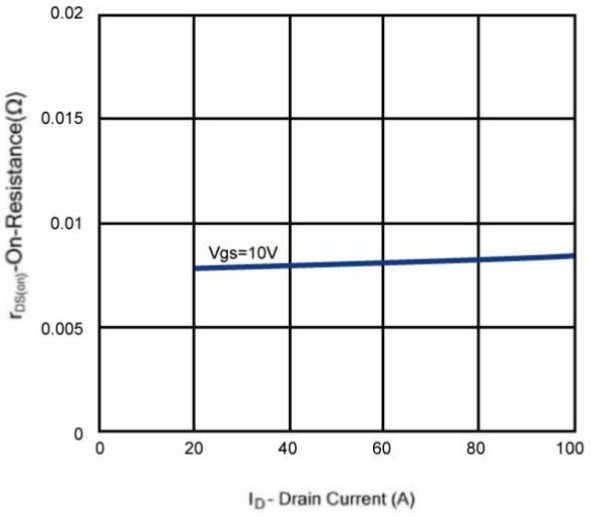
Typical Characteristics (T_J =25℃ Noted)

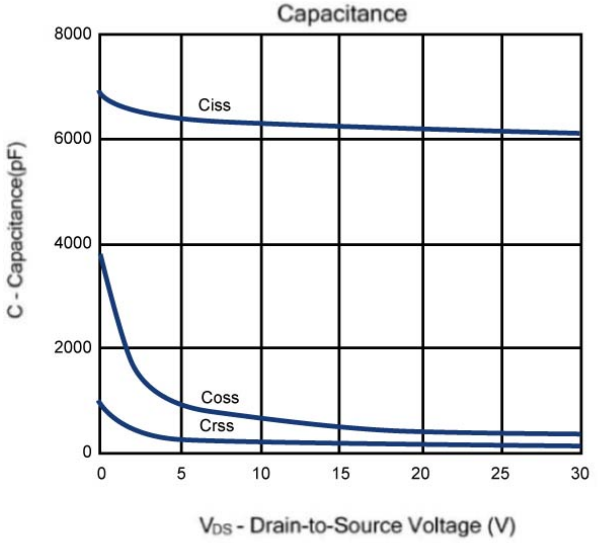
On Resistance vs. Junction Temperature



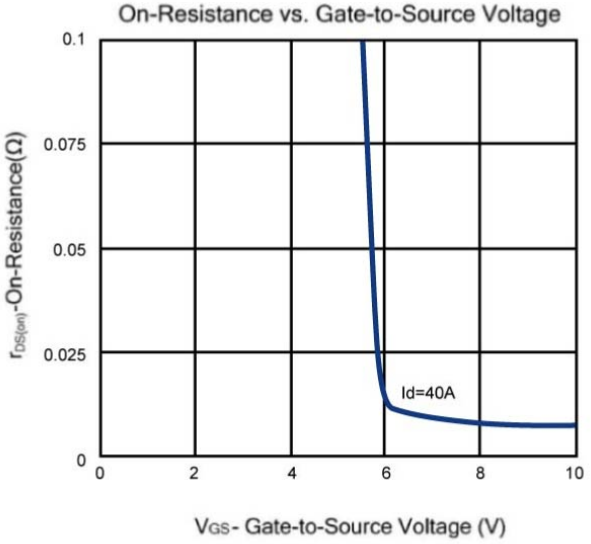
On-Resistance vs. Drain Current



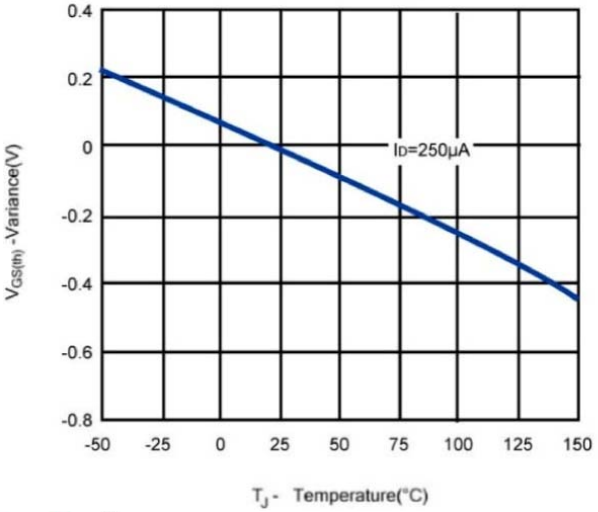
Capacitance



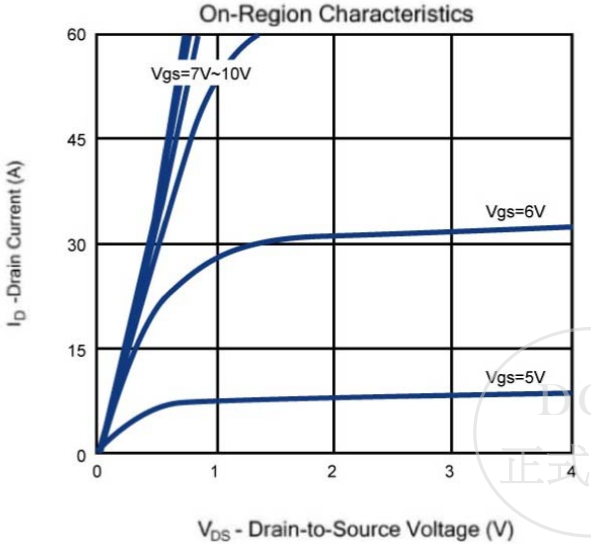
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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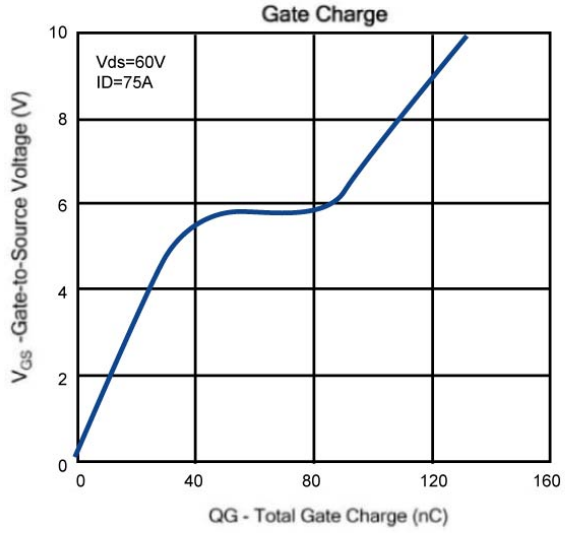
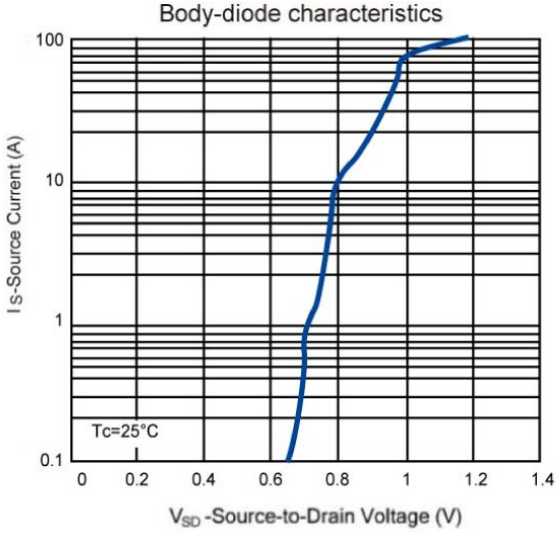
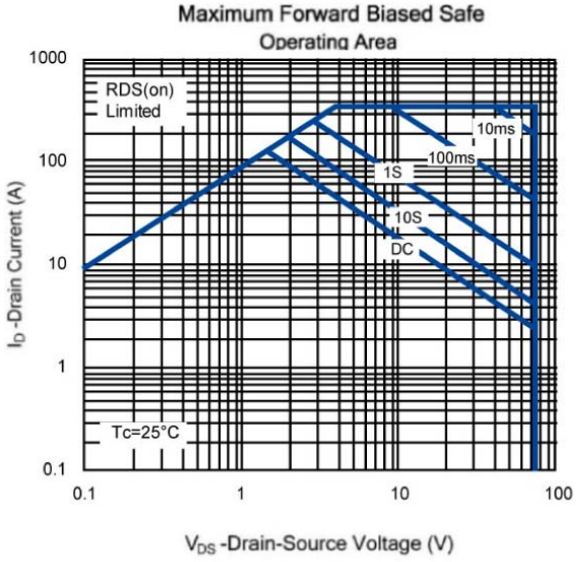
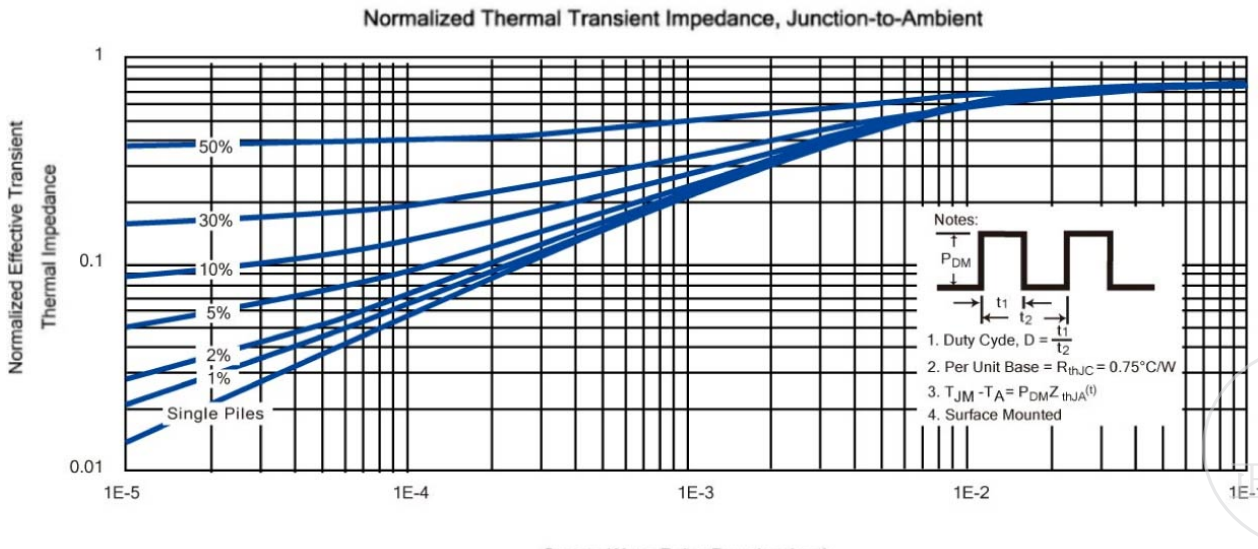
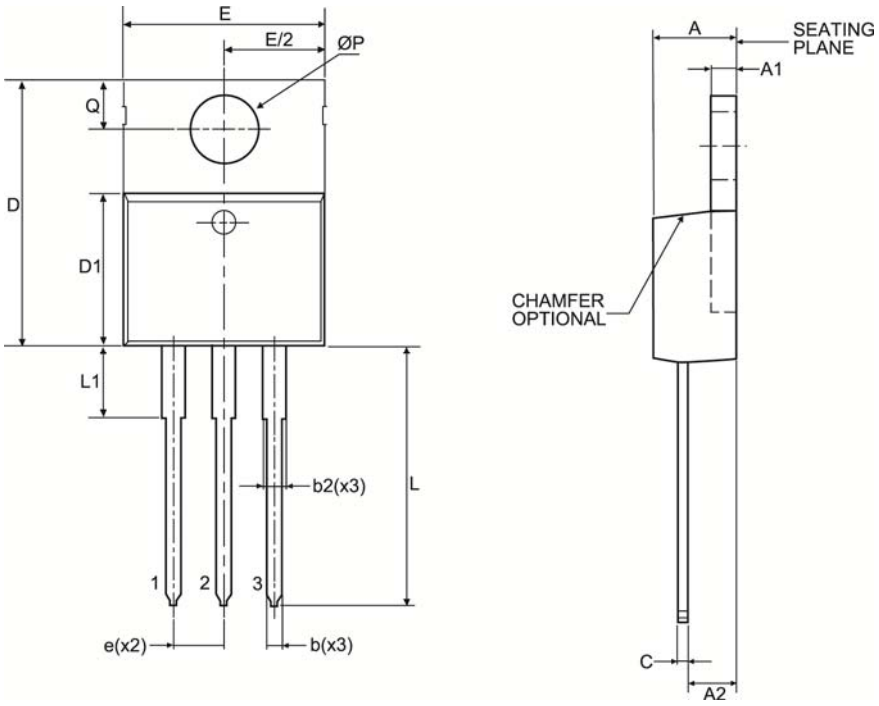








TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20