

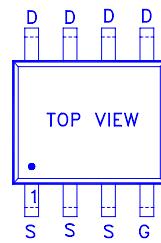
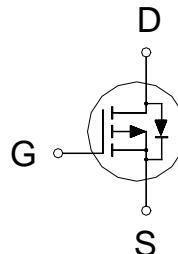
NIKO-SEM
**P-Channel Logic Level Enhancement
Mode Field Effect Transistor**
P2003EVG

SOP-8

Lead-Free

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30	20m	-9A


 4 :GATE
 5,6,7,8 :DRAIN
 1,2,3 :SOURCE
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNITS
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	± 20		V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	-9		A
	$T_C = 70^\circ\text{C}$		-8		
Pulsed Drain Current ¹		I_{DM}	-50		
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	2.5		W
	$T_C = 70^\circ\text{C}$		1.3		
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		25	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	°C / W

¹Pulse width limited by maximum junction temperature.²Duty cycle $\leq 1\%$ **ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-30			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -10V$	-50			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -4.5V, I_D = -7\text{A}$		25	35	$\text{m}\Omega$
		$V_{GS} = -10V, I_D = -9\text{A}$		15	20	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -10V, I_D = -9\text{A}$		24		S

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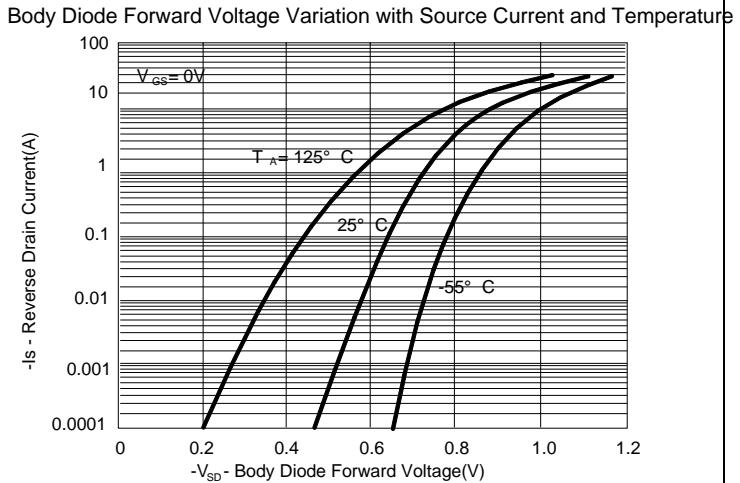
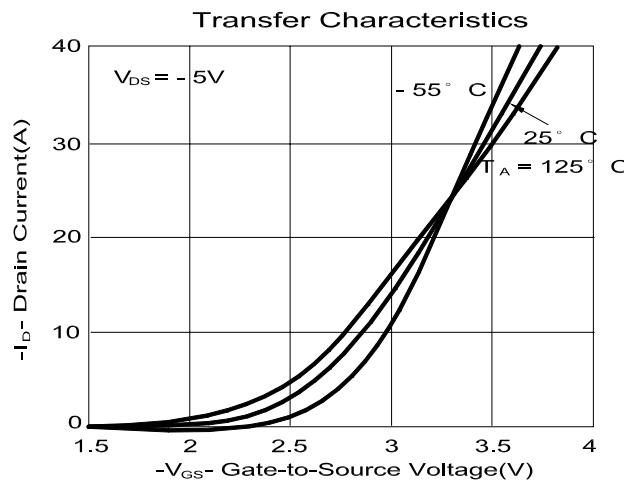
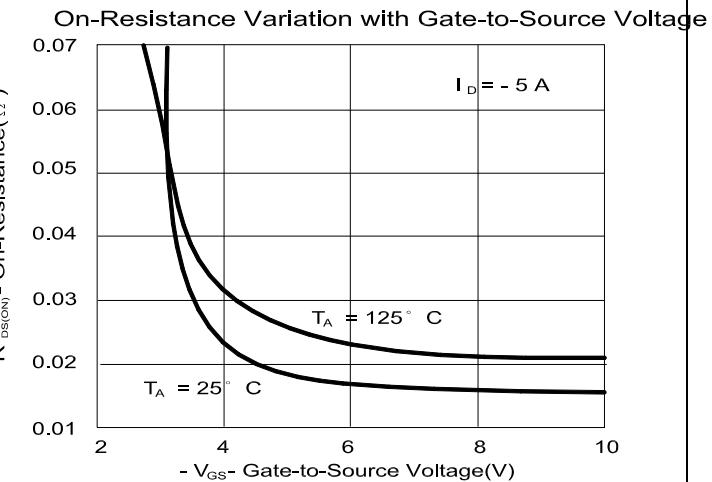
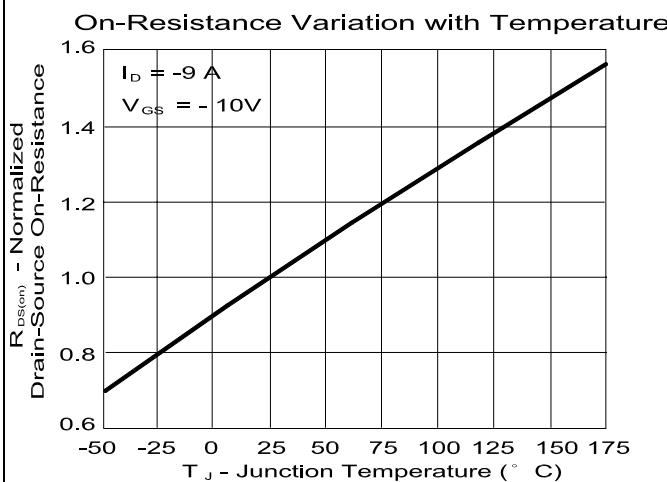
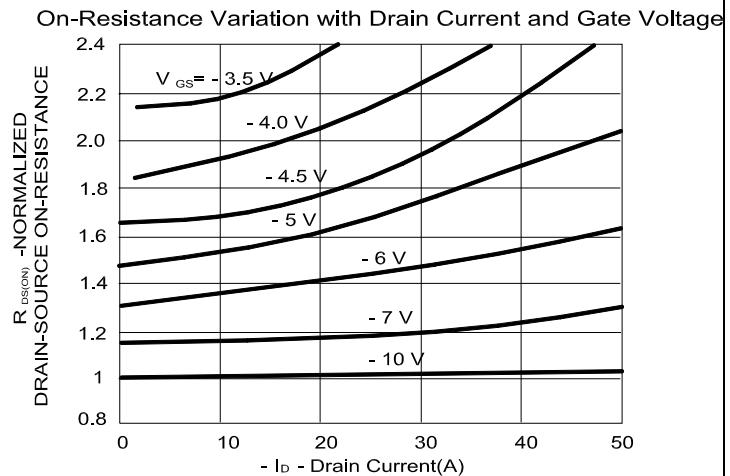
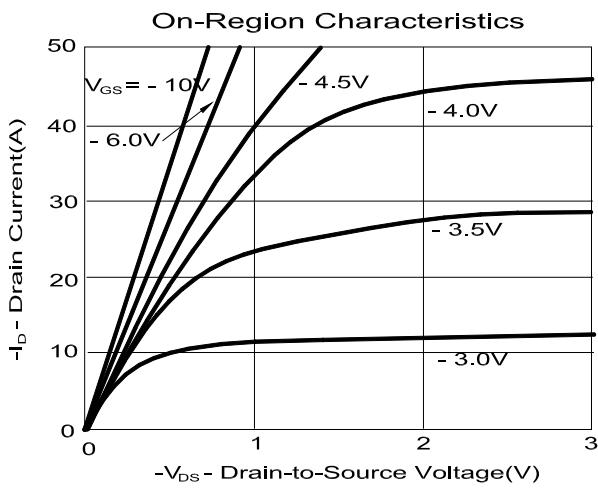
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DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	1610			pF
Output Capacitance	C_{oss}		410			
Reverse Transfer Capacitance	C_{rss}		200			
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V,$ $I_D = -9A$	17	24		nC
Gate-Source Charge ²	Q_{gs}		5			
Gate-Drain Charge ²	Q_{gd}		6			
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = -15V, R_L = 1$ $I_D \geq -1A, V_{GS} = -10V, R_{GS} = 6$	5.7			nS
Rise Time ²	t_r		10			
Turn-Off Delay Time ²	$t_{d(off)}$		18			
Fall Time ²	t_f		5			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ C$)						
Continuous Current	I_S				-2.1	A
Pulsed Current ³	I_{SM}				-4	
Forward Voltage ¹	V_{SD}	$I_F = -1A, V_{GS} = 0V$			-1.2	V

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.**REMARK: THE PRODUCT MARKED WITH “P2003EVG”, DATE CODE or LOT #**

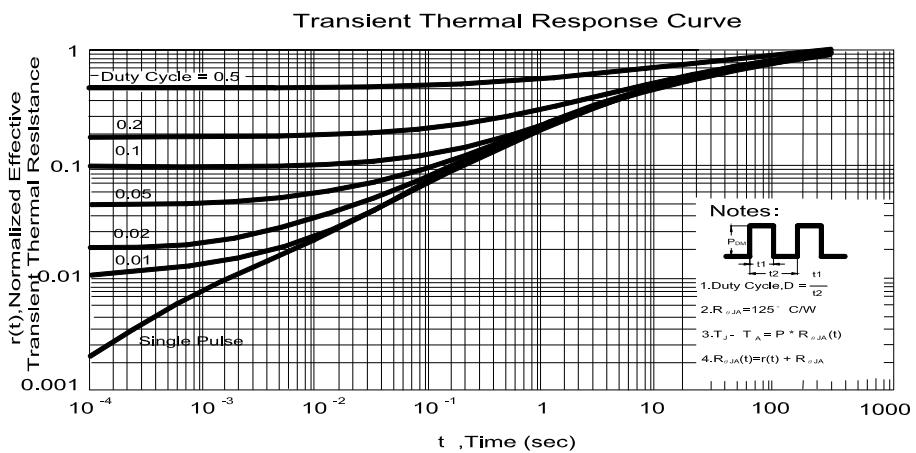
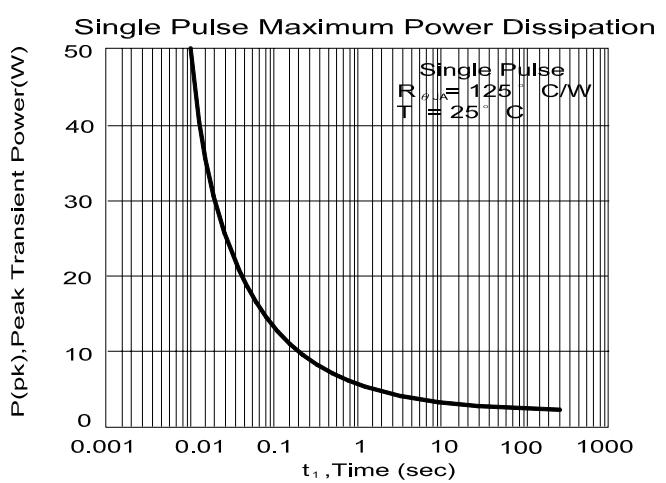
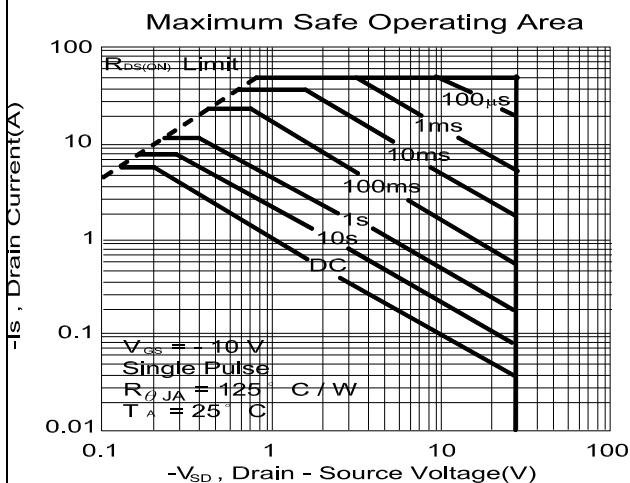
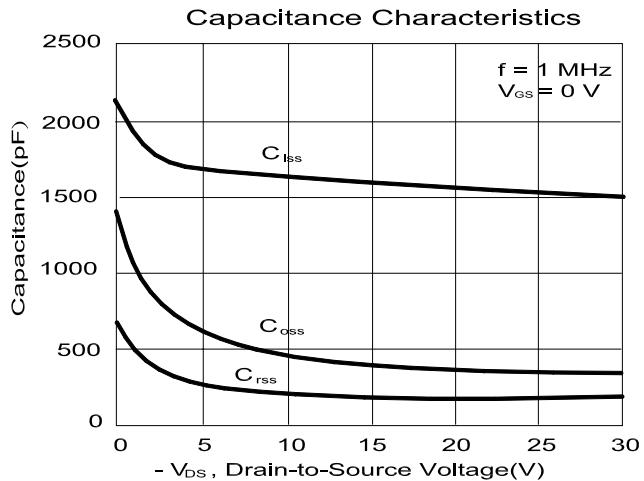
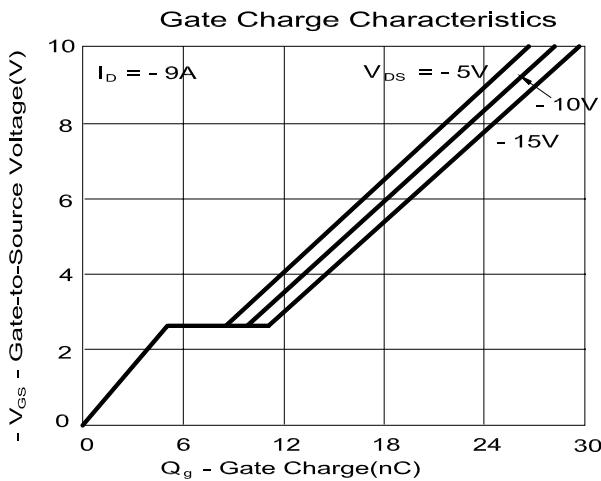
Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.

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SOIC-8(D) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.5	0.715	0.83
B	3.8	3.9	4.0	I	0.18	0.254	0.25
C	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	K	0°	4°	8°
E		1.27		L			
F	1.35	1.55	1.75	M			
G	0.1	0.175	0.25	N			

