N- and P-Channel 40-V (D-S) MOSFET

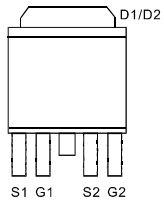
General Description

The B3965D is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits with high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- **40V/5.2A, $R_{DS(ON)}$=40mΩ@V_{GS}=10V (N-Ch)**
- **40V/4.9A, $R_{DS(ON)}$=45mΩ@V_{GS}=4.5V (N-Ch)**
- **-40V/-4.5A, $R_{DS(ON)}$=54mΩ@V_{GS}=-10V (P-Ch)**
- **-40V/-3.9A, $R_{DS(ON)}$=72mΩ@V_{GS}=-4.5V (P-Ch)**
- **Super High Density Cell Design For Extremely Low $R_{DS(ON)}$)**
- **Exceptional On-Resistance and Maximum DC Current Capability**
- **TO-252 Package**

Pin Configuration



Applications

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

Absolute Maximum Ratings (TA=25℃ Unless Otherwise Noted):

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current(tJ=150℃)	TA=25℃	I_D	6.9	-6.1	A
	TA=70℃		5.5	-4.9	
Pulsed Drain Current		I_{DM}	30	-30	A
Continuous Source Current (Diode Conduction)		I_S	1.7	-1.7	A
Avalanche Energy with Single Pulse(L=0.1mH)		E_{AS}	10	20	mJ
Maximum Power Dissipation	TA=25℃	P_D	2.0		W
	TA=70℃		1.3		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		RθJA	Steady 75	Steady 65	℃/W
			10sec 47	10sec 35	
Thermal Resistance-Junction to Case		RθJC	44	30	℃/W