

## SWITCHING REGULATOR APPLICATIONS

## Features

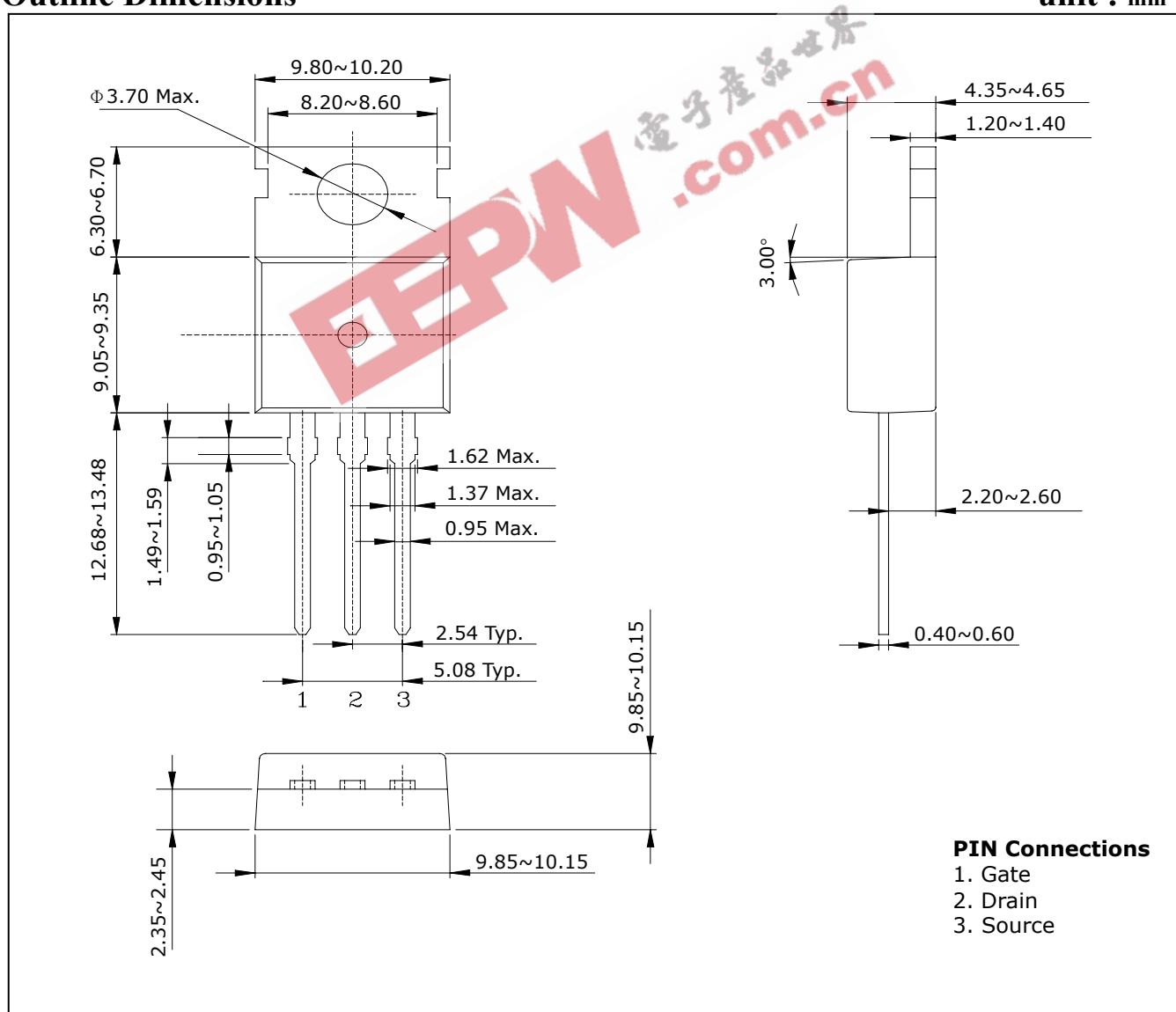
- High Voltage:  $BV_{DSS}=500V$ (Min.)
  - Low  $C_{rss}$  :  $C_{rss}=12pF$ (Typ.)
  - Low gate charge :  $Qg=28nC$ (Typ.)
  - Low  $R_{DS(on)}$  :  $R_{DS(on)}=0.8\Omega$ (Max.)

## **Ordering Information**

Type NO.	Marking	Package Code
STK0850P	STK0850	TO-220AB-3L

## Outline Dimensions

unit : mm



**Absolute maximum ratings**(T<sub>c</sub>=25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V <sub>DSS</sub>	500	V
Gate-source voltage	V <sub>GSS</sub>	±30	V
Drain current (DC)	I <sub>D</sub>	(T <sub>c</sub> =25°C)	8
		(T <sub>c</sub> =100°C)	3.9
Drain current (Pulsed) *	I <sub>DM</sub>	32	A
Drain power dissipation	P <sub>D</sub>	65	W
Avalanche current (Single) ②	I <sub>AS</sub>	8	A
Single pulsed avalanche energy ②	E <sub>AS</sub>	360	mJ
Avalanche current (Repetitive) ①	I <sub>AR</sub>	8	A
Repetitive avalanche energy ①	E <sub>AR</sub>	7.5	mJ
Junction temperature	T <sub>J</sub>	150	°C
Storage temperature range	T <sub>stg</sub>	-55~150	

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max	Unit
Thermal resistance	R <sub>th(J-C)</sub>	-	1.92	°C/W
	R <sub>th(J-a)</sub>	-	83.3	

**Electrical Characteristics**

(Tc=25°C)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0	500	-	-	V
Gate threshold voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA, V <sub>DS</sub> = V <sub>GS</sub>	2.0	-	4.0	V
Drain-source cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> =500V, V <sub>GS</sub> =0V	-	-	1	μA
Gate leakage current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA
Drain-source on-resistance ④	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =4.0A	-	0.65	0.8	Ω
Forward transfer conductance ④	g <sub>fs</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =4.0A	-	6.5	-	S
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz	-	950	1430	pF
Output capacitance	C <sub>oss</sub>		-	100	150	
Reverse transfer capacitance	C <sub>rss</sub>		-	12	18	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =200V, I <sub>D</sub> =8A R <sub>G</sub> =25Ω	-	18	-	ns
Rise time	t <sub>r</sub>		-	65	-	
Turn-off delay time	t <sub>d(off)</sub>		-	93	-	
Fall time	t <sub>f</sub>		-	64	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> =200V, V <sub>GS</sub> =10V I <sub>D</sub> =8A	-	28	42	nC
Gate-source charge	Q <sub>gs</sub>		-	5	8	
Gate-drain charge	Q <sub>gd</sub>		-	10	15	

**Source-Drain Diode Ratings and Characteristics**

(Tc=25°C)

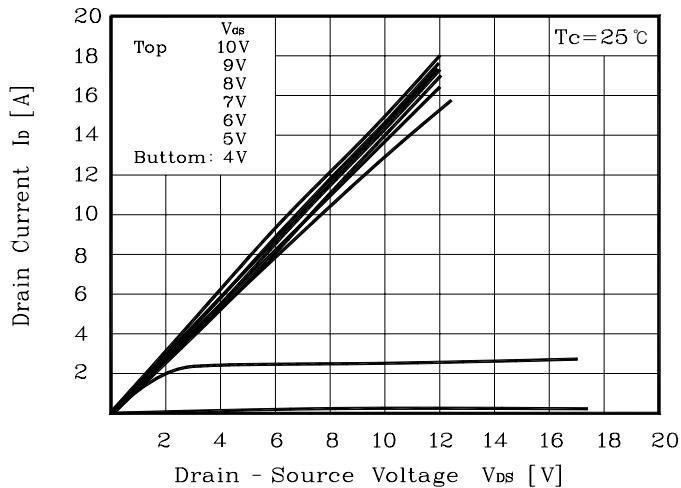
Characteristic	Symbol	Test Condition	Min	Typ	Max	Units
Continuous source current	I <sub>s</sub>	Integral reverse diode in the MOSFET	-	-	8	A
Pulsed-source current ①	I <sub>SM</sub>		-	-	32	
Forward voltage ④	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>s</sub> =8A	-	-	1.4	V
Reverse recovery time	t <sub>rr</sub>	I <sub>s</sub> =8A, V <sub>GS</sub> =0 dI <sub>s</sub> /dt=100A/us	-	335	-	ns
Reverse recovery charge	Q <sub>rr</sub>		-	4.55	-	uC

Note :

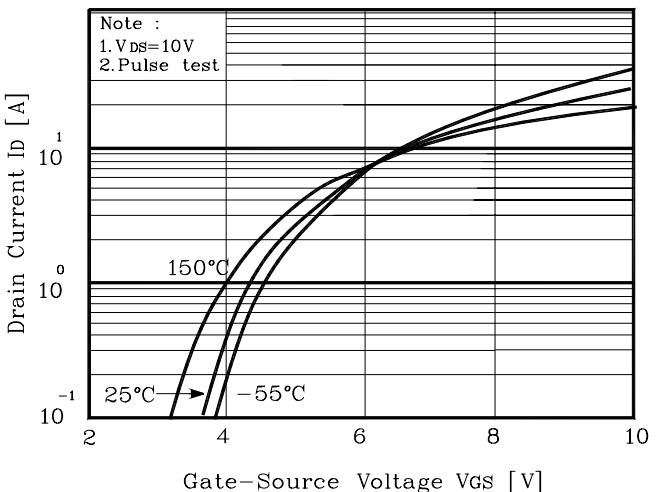
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② L=10mH, I<sub>AS</sub>=8A, V<sub>DD</sub>=50V, R<sub>G</sub>=27Ω , starting T<sub>j</sub>=25 °C
- ③ Pulse Test : Pulse Width < 300us, Duty cycle≤ 2%
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

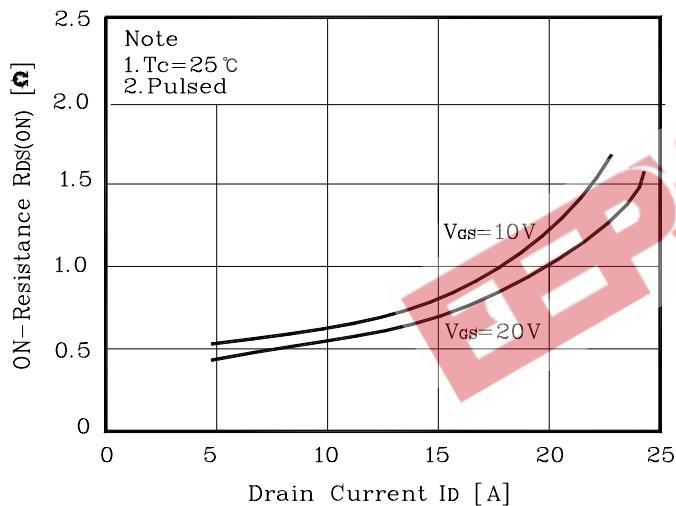
**Fig. 1  $I_D$  -  $V_{DS}$**



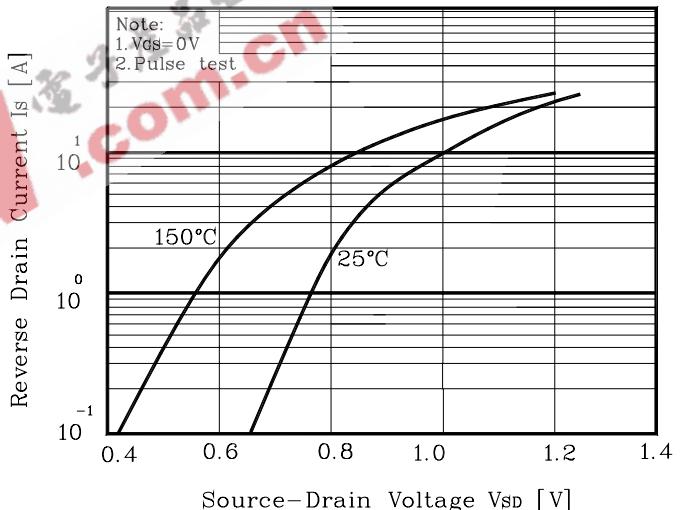
**Fig. 2  $I_D$  -  $V_{GS}$**



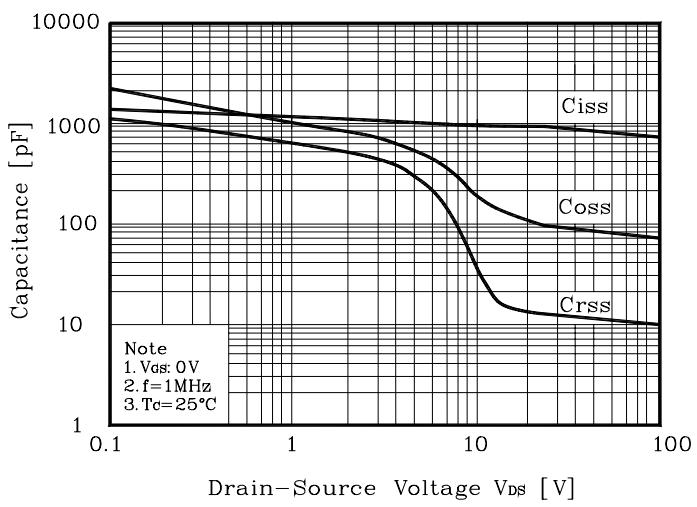
**Fig. 3  $R_{DS(on)}$  -  $I_D$**



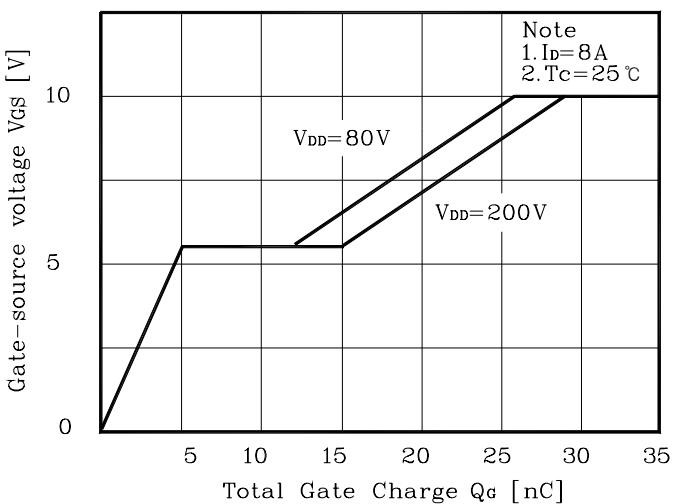
**Fig. 4  $I_S$  -  $V_{SD}$**



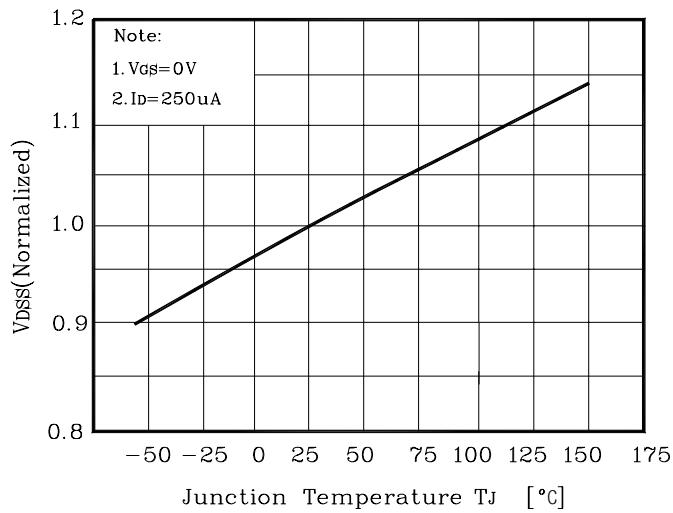
**Fig. 5 Capacitance -  $V_{DS}$**



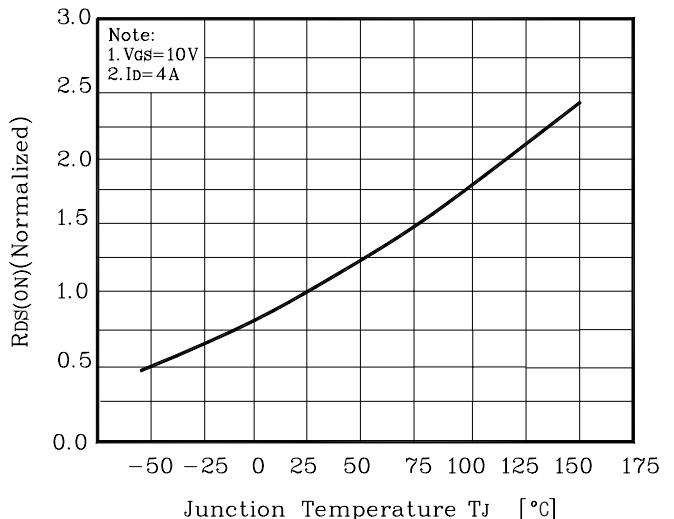
**Fig. 6  $V_{GS}$  -  $Q_G$**



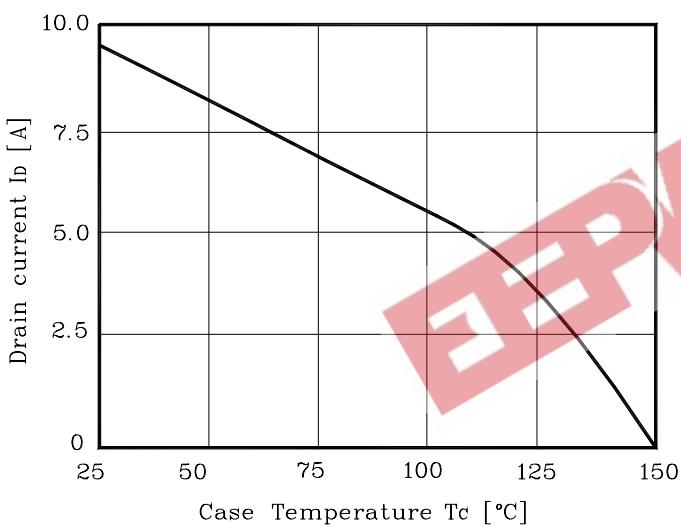
**Fig. 7  $V_{DSS}$  -  $T_J$**



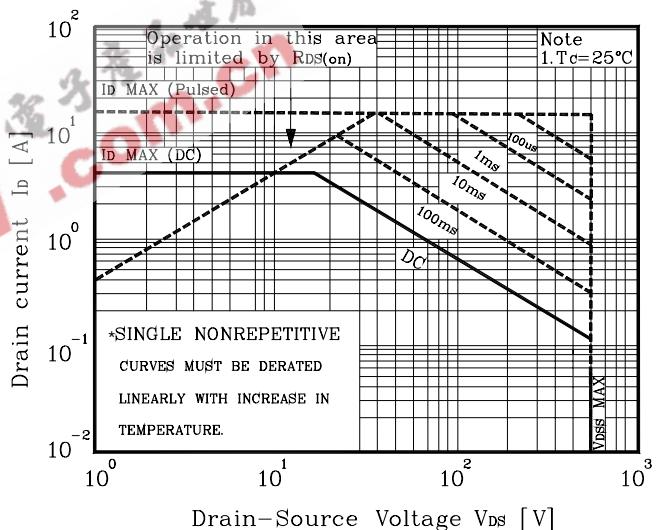
**Fig.8  $R_{DS(on)}$  -  $T_J$**



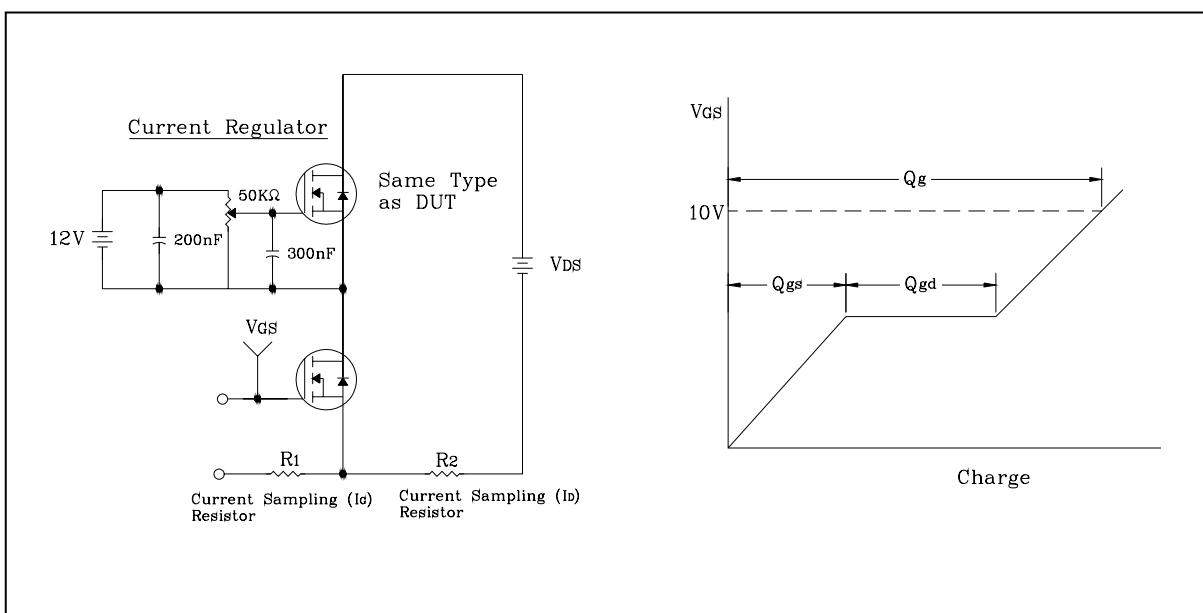
**Fig. 9  $I_D$  -  $T_C$**



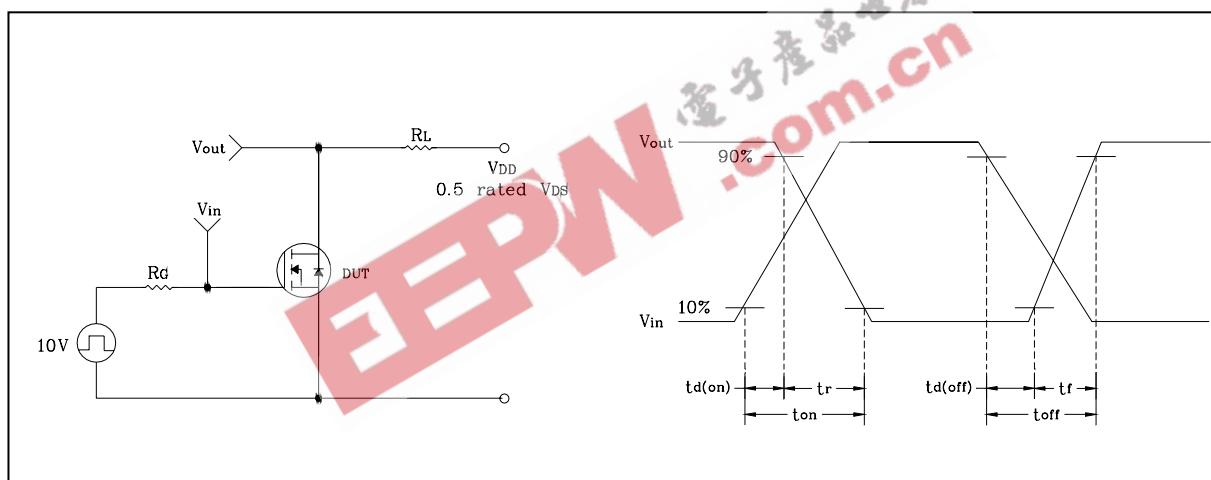
**Fig. 10 Safe Operating Area**



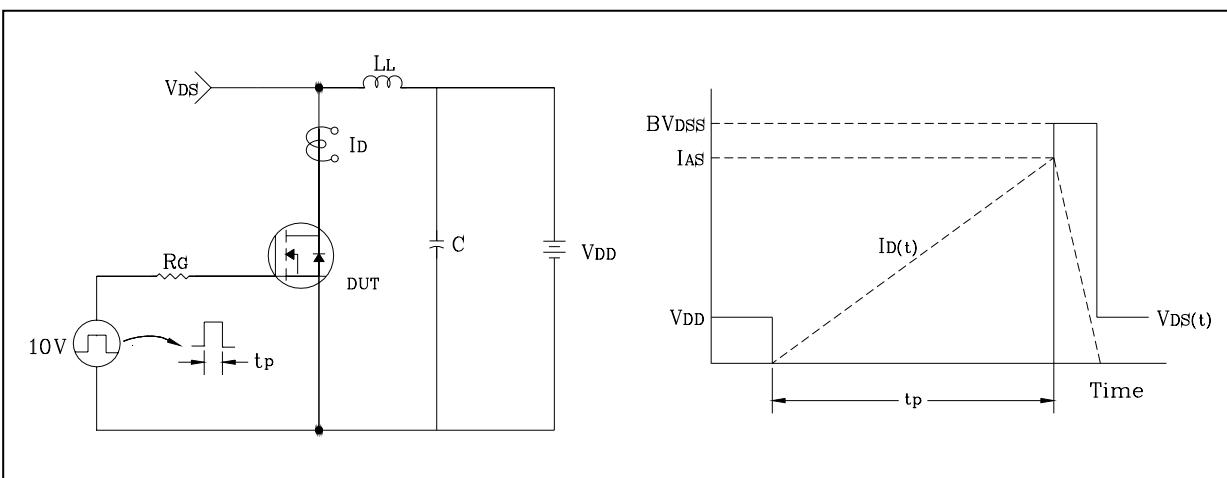
**Fig. 10 Gate Charge Test Circuit & Waveform**



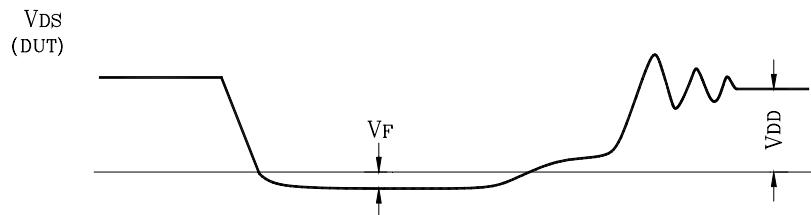
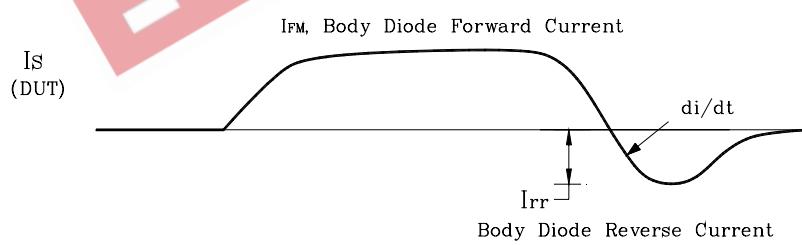
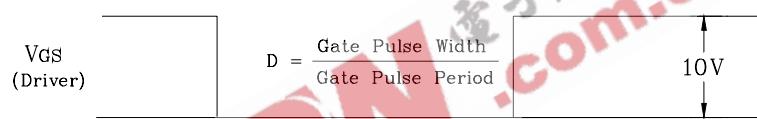
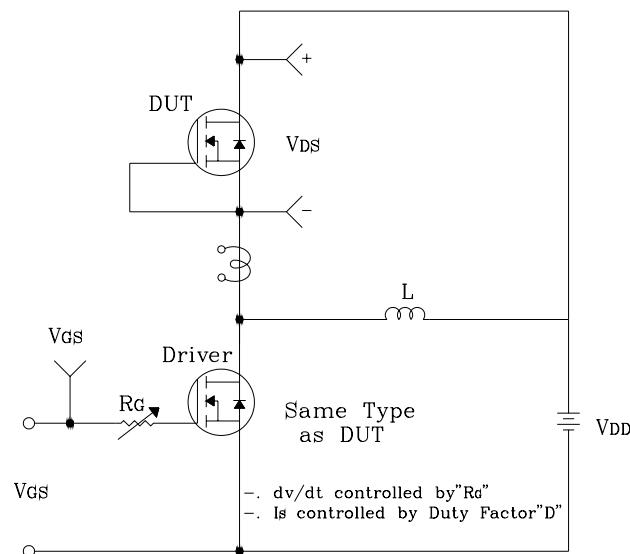
**Fig. 11 Resistive Switching Test Circuit & Waveform**



**Fig. 12 E<sub>AS</sub> Test Circuit & Waveform**



**Fig. 13 Diode Reverse Recovery Time Test Circuit & Waveform**





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