



## AOD413 P-Channel Enhancement Mode Field Effect Transistor

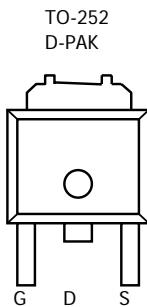


### General Description

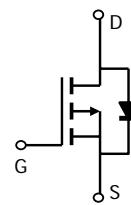
The AOD413 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications. *Standard Product AOD413 is Pb-free (meets ROHS & Sony 259 specifications). AOD413L is a Green Product ordering option. AOD413 and AOD413L are electrically identical.*

### Features

$V_{DS} (V) = -40V$   
 $I_D = -12A (V_{GS} = -10V)$   
 $R_{DS(ON)} < 45m\Omega (V_{GS} = -10V)$   
 $R_{DS(ON)} < 69m\Omega (V_{GS} = -4.5V)$



Top View  
Drain Connected to Tab



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,G</sup>	$I_D$	-12	A
$T_A=100^\circ C$ <sup>G</sup>		-12	
Pulsed Drain Current	$I_{DM}$	-30	
Avalanche Current <sup>C</sup>	$I_{AR}$	-12	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	30	mJ
Power Dissipation <sup>B</sup>	$P_D$	50	W
$T_C=100^\circ C$		25	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2.5	W
$T_A=70^\circ C$		1.6	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	°C

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16.7	25	°C/W
Maximum Junction-to-Ambient <sup>A</sup>		40	50	°C/W
Maximum Junction-to-Case <sup>C</sup>	$R_{\theta JL}$	2.5	3	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$I_D=-10\text{mA}$ , $V_{GS}=0\text{V}$	-40			V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS}=-32\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_D=-250\mu\text{A}$	-1	-1.9	-3	V
$I_{\text{D(ON)}}$	On state drain current	$V_{GS}=-10\text{V}$ , $V_{DS}=-5\text{V}$	-30			A
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$ , $I_D=-12\text{A}$ $T_J=125^\circ\text{C}$		36 56	45 70	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$ , $I_D=-8\text{A}$		51	69	$\text{m}\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-12\text{A}$		16		S
$V_{\text{SD}}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.75	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-12	A
<b>DYNAMIC PARAMETERS</b>						
$C_{\text{iss}}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-20\text{V}$ , $f=1\text{MHz}$		657	850	pF
$C_{\text{oss}}$	Output Capacitance			143	185	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance			63	90	pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		6.5		$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$ , $V_{DS}=-20\text{V}$ , $I_D=-12\text{A}$		14.1		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			7		nC
$Q_{\text{gs}}$	Gate Source Charge			2.2		nC
$Q_{\text{gd}}$	Gate Drain Charge			4.1		nC
$t_{\text{D(on)}}$	Turn-On DelayTime	$V_{GS}=-10\text{V}$ , $V_{DS}=-20\text{V}$ , $R_L=1.7\Omega$ , $R_{\text{GEN}}=3\Omega$		8		ns
$t_r$	Turn-On Rise Time			12.2		ns
$t_{\text{D(off)}}$	Turn-Off DelayTime			24		ns
$t_f$	Turn-Off Fall Time			12.5		ns
$t_{\text{rr}}$	Body Diode Reverse Recovery Time	$I_F=-12\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		23.2		ns
$Q_{\text{rr}}$	Body Diode Reverse Recovery Charge	$I_F=-12\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		18.2		nC

A: The value of  $R_{\text{qJA}}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation PSDM is based on  $R_{\text{qJA}}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B. The power dissipation PD is based on  $T_J(\text{MAX})=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_J(\text{MAX})=175^\circ\text{C}$ .

D. The  $R_{\text{qJA}}$  is the sum of the thermal impedance from junction to case  $R_{\text{qJC}}$  and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using  $<300\text{ ms}$  pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_J(\text{MAX})=175^\circ\text{C}$ .

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

Rev 3: Jan 2006

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

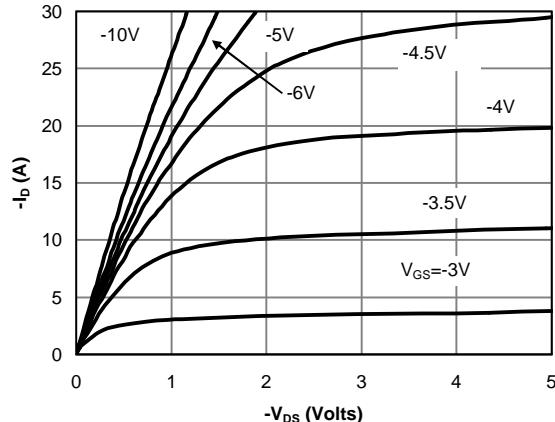


Fig 1: On-Region Characteristics

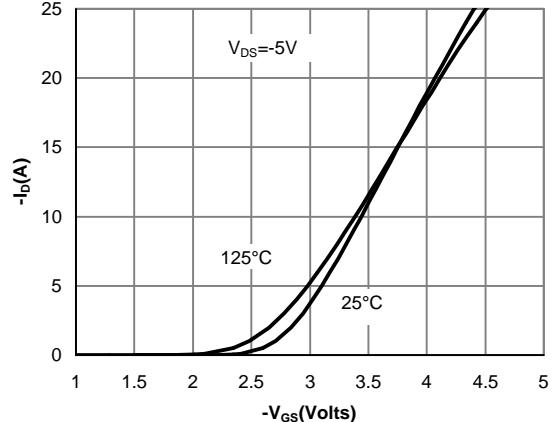


Figure 2: Transfer Characteristics

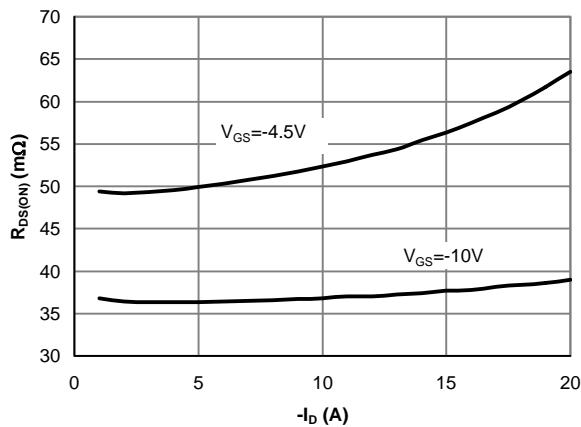


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

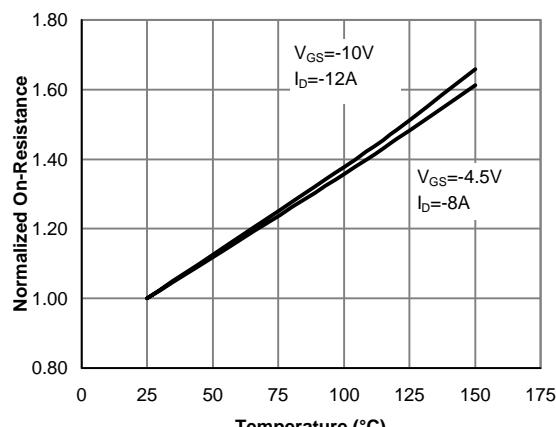


Figure 4: On-Resistance vs. Junction Temperature

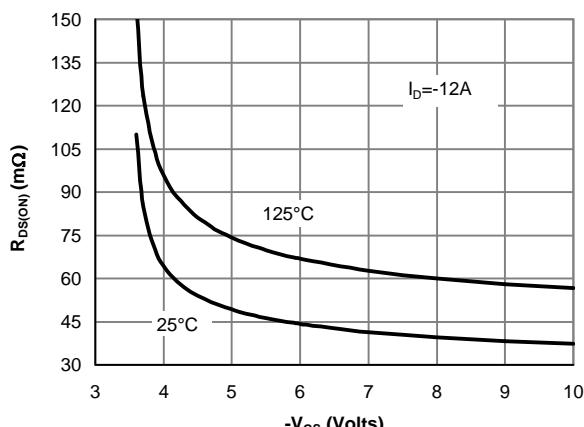


Figure 5: On-Resistance vs. Gate-Source Voltage

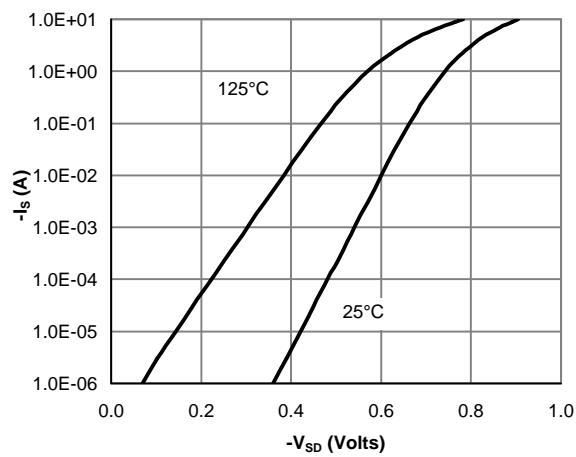


Figure 6: Body-Diode Characteristics

---

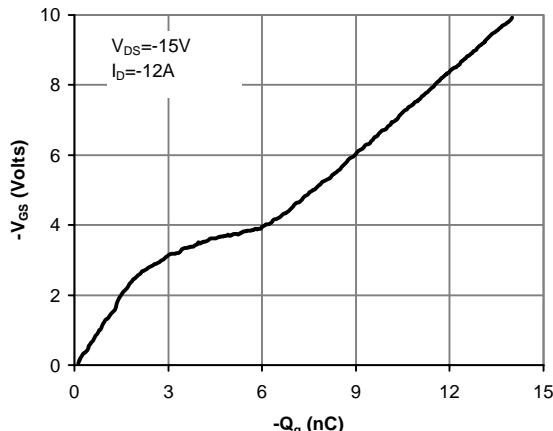
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**


Figure 7: Gate-Charge Characteristics

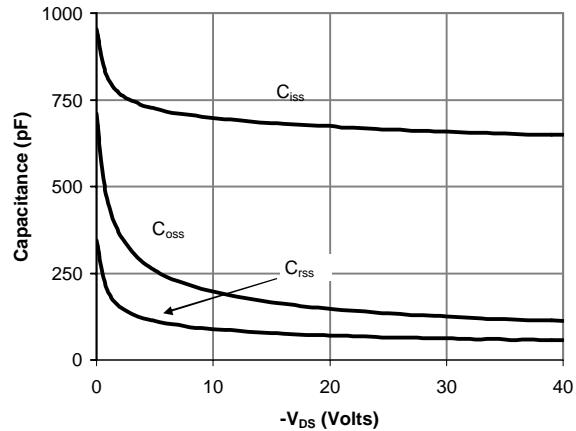


Figure 8: Capacitance Characteristics

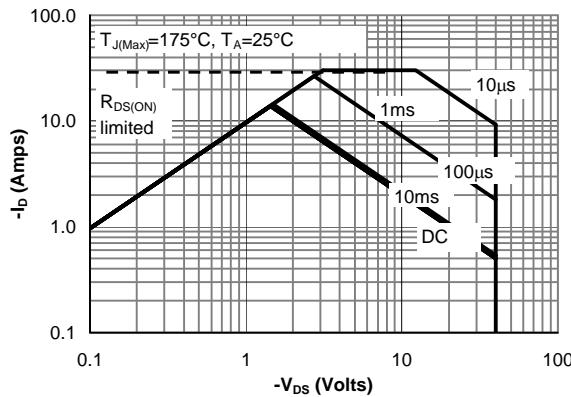


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

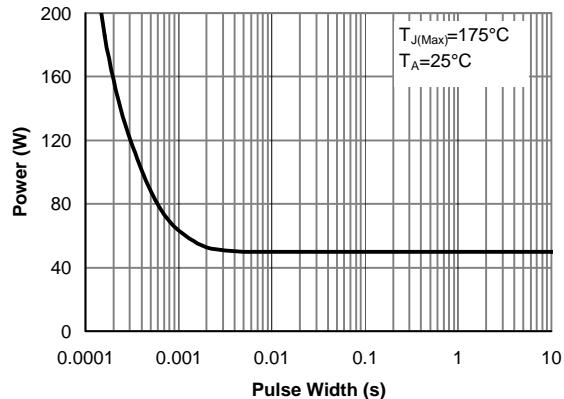


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

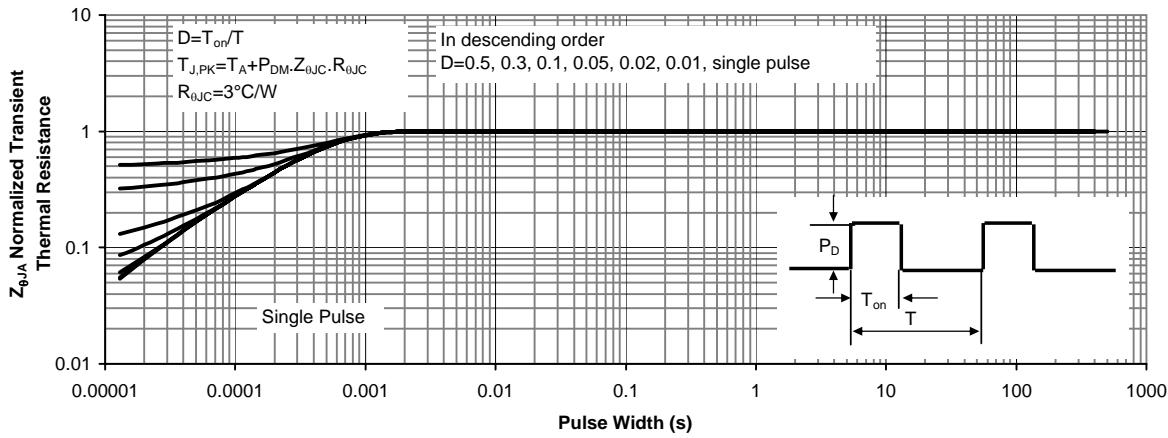


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

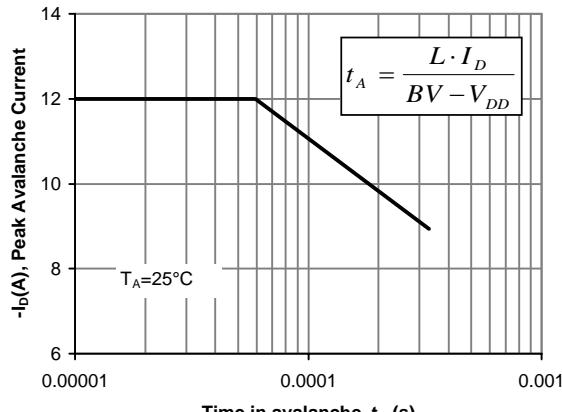


Figure 12: Single Pulse Avalanche capability

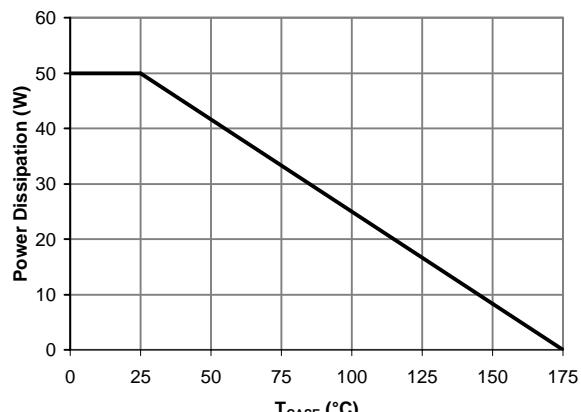


Figure 13: Power De-rating (Note B)

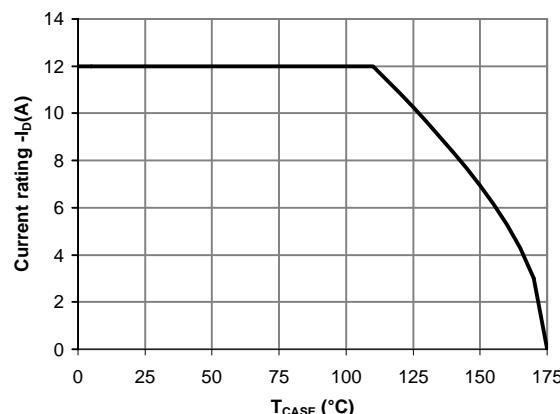


Figure 14: Current De-rating (Note B)

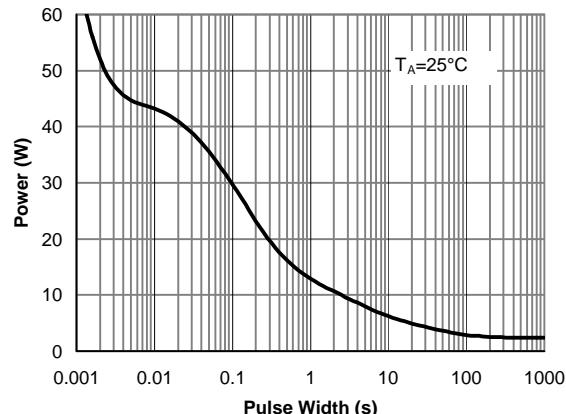


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

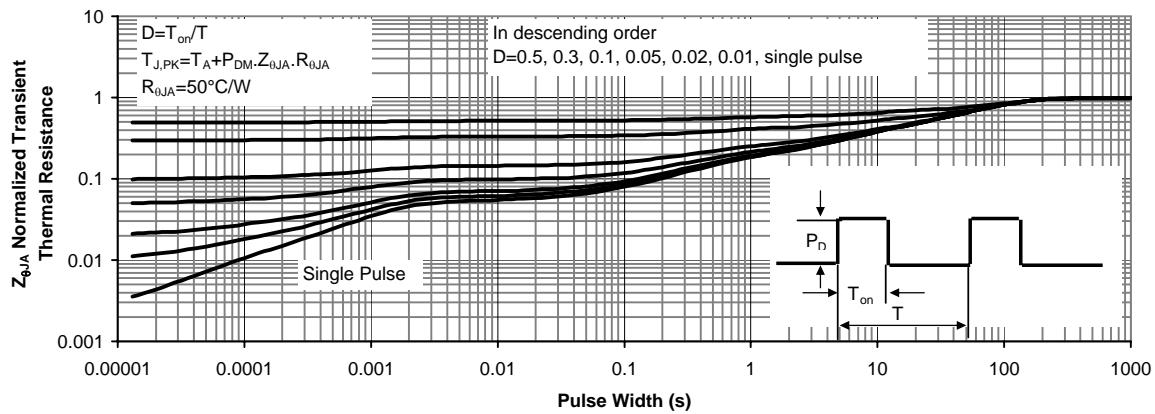


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)