R2A20133DSP

Critical Conduction Mode PFC Control IC

R03DS0052EJ0100
Rev.1.00
Dec 19, 2011

Description

The R2A20133D controls a boost converter to provide an active power factor correction.

The R2A20133D adopts critical conduction mode for power factor correction and realizes high efficiency and a low switching noise by zero current switching.

Because the zero current is detected by using the GND current, the ZCD Auxiliary winding is unnecessary.

The feedback loop open detection, two mode overvoltage protection, overcurrent protection are built in the R2A20133D, and can constitute a power supply system of high reliability with few external parts.

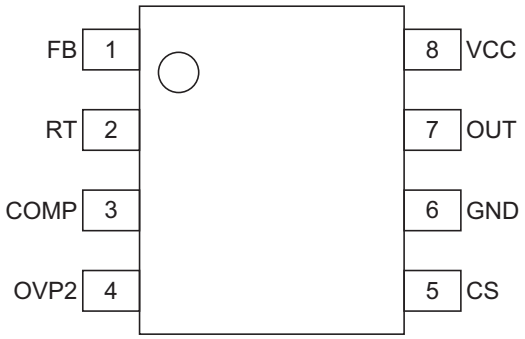
Features

- Absolute Maximum Ratings
  - Supply voltage Vcc: 24 V
  - Operating junction temperature Tjopr: –40 to +150°C
- Electrical characteristics
  - UVLO operation start voltage VH: 9.5 V ± 0.7 V
  - UVLO operation shutdown voltage VL: 8.5 V ± 0.4 V
  - UVLO hysteresis voltage Hysuvl: 1.0 V ± 0.4 V
- Functions
  - Boost converter control with critical conduction mode
  - Two mode overvoltage protection and OVP2
    Mode 1: Dynamic OVP corresponding to a voltage rise by load change
    Mode 2: Static OVP corresponding to overvoltage in stable.
    OVP2: OVP2 senses the PFC output voltage by independence pin.
  - Feedback loop, open detection
  - Overcurrent protection
  - Dynamic UVP corresponding to a voltage fall by load change
  - Frequency limiter, adjustable
  - Zero Current Detect (ZCD) delay time, adjustable
  - CS pin's open detection
  - Package lineup: Pb-free SOP-8 (JEDEC)

Ordering Information

Part No.	Package Name	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
R2A20133DSP#W5	—	PRSP0008DJ-A	SP	W (2,500 pcs/reel)

Pin Arrangement

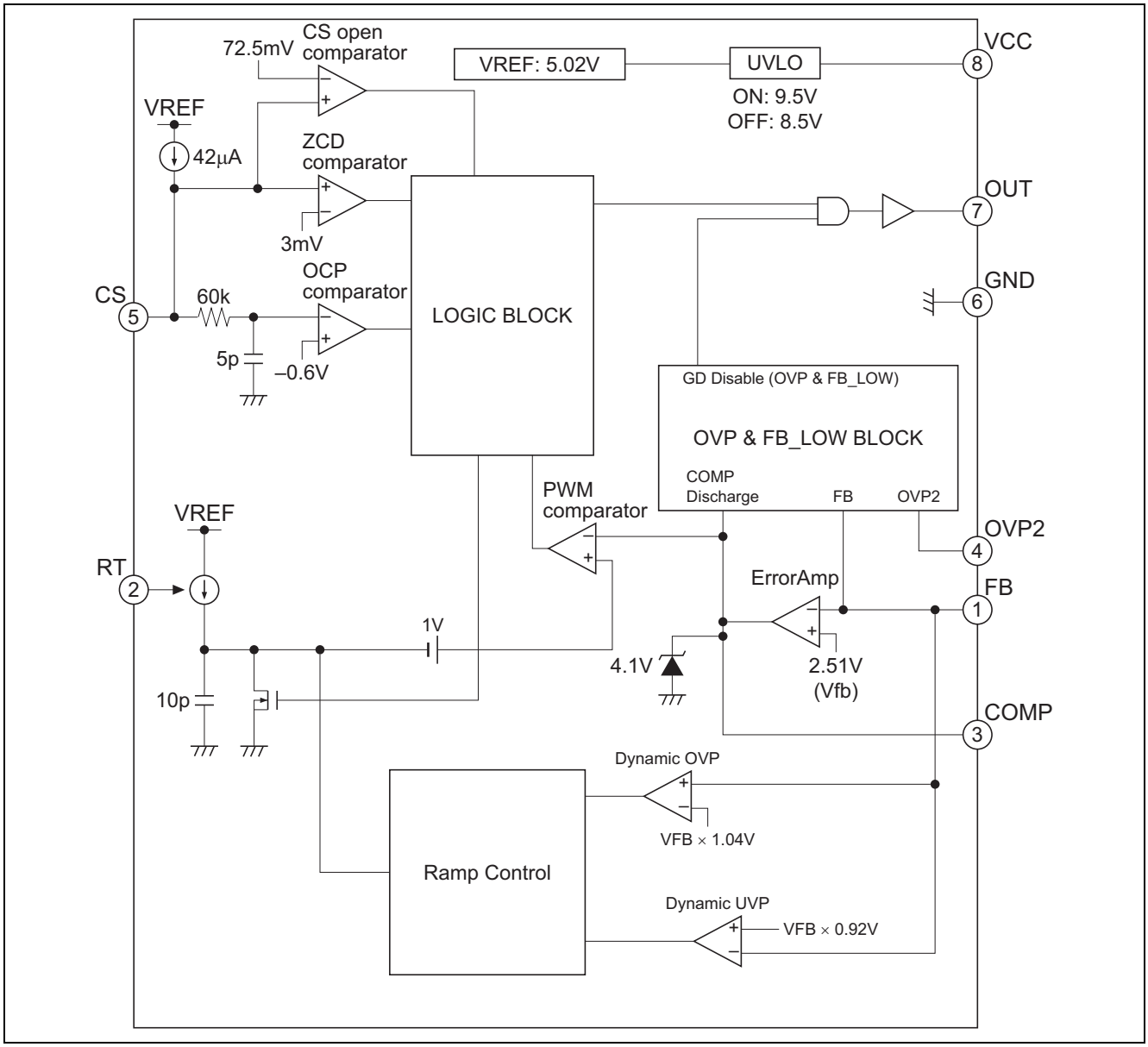


(Top view)

Pin Functions

Pin No.	Pin Name	Function
1	FB	Error amplifier input terminal
2	RT	Max-ON time, ZCD-delay and Frequency limiter adjustment terminal
3	COMP	Error amplifier output terminal
4	OVP2	Over voltage detection terminal
5	CS	Zero current detection and overcurrent detection input terminal
6	GND	Ground
7	OUT	Power MOSFET drive terminal
8	VCC	Supply voltage terminal

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	VCC	–0.3 to +24	V	
OUT terminal peak current	Ipk-snk-out Ipk-src-out	+0.9 –0.5	A	3
OUT terminal DC current	Idc-snk-out Idc-src-out	+100 –50	mA	
COMP terminal current	Icomp	+1 –1	mA	
RT terminal current	Irt	–50 to –2	μA	
Terminal voltage	Vt-group1	–0.3 to VCC	V	4
	Vt-group2	–0.3 to 5.3		5
CS terminal voltage	Vcs	–5 to +0.3	V	
Power dissipation	Pt	0.68	W	6
Operating junction temperature	Tj-opr	–40 to +150	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are with reference to the GND terminal.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. Shows the transient current when driving a capacitive load.
4. This is the rated voltage for the following pins:
   OUT
5. This is the rated voltage for the following pins:
   FB, COMP, OVP2, RT
6. θja = 120°C/W
   This value is a thing mounting on 40 × 40 × 1.6 [mm], a glass epoxy board of wiring density 10%.

Electrical Characteristics

(Ta = 25°C, VCC = 12 V, CS = 0.04 V, FB = 2 V, COMP: Open, OVP2 = 1 V, RRT = 200 kΩ)

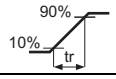
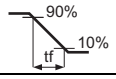
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	8.8	9.5	10.2	V	
	UVLO turn-off threshold	Vuvll	8.1	8.5	8.9	V	
	UVLO hysteresis	Hysuvl	0.6	1.0	1.4	V	
	Standby current	Istby	—	100	200	μA	VCC = Vuvlh – 0.2 V
	Operating current	Icc	—	1.8	2.6	mA	
Error amplifier	Feedback voltage	Vfb	2.472	2.510	2.548	V	FB-COMP short
	Temperature stability	dVfb	—	±80	—	ppm/°C	Ta = –40 to +125°C *1
	Input bias current	Ifb	–0.40	–0.15	–0.05	μA	Measured pin: FB
	Open loop gain	Av	—	65	—	dB	*1
	Upper clamp voltage	Vclamp-comp	3.75	4.10	4.35	V	FB = 2.45 V COMP: Open
	Low voltage	Vl-comp	—	0.1	0.3	V	FB = 3.0 V COMP: Open
	Source current1	Isrc-comp1	–13.5	–10	–6	μA	FB = 1.7 V COMP = 2.5 V
	Source current2	Isrc-comp2	Isrc-comp1 ×3.3	Isrc-comp1 ×3.0	Isrc-comp1 ×2.7	μA	FB = 1.5 V COMP = 2.5 V
	Sink current	Isnk-comp	6	10	13.5	μA	FB = 3.5 V COMP = 2.5 V
	Transconductance	gm	25	46	75	μS	FB = 2.45V ↔ 2.55 V COMP = 2.5 V
RT	RAMP offset voltage	Voff_ramp	—	1.0	—	V	*1
	RAMP amplitude	dVramp	2.90	3.1	3.3	V	*2
	RT voltage	V-rt	2.5	2.6	2.7	V	
	ZCD delay time	Zcd-delay	—	0.87	—	μs	RRT = 200 kΩ *1
	Maximum frequency	fmax	—	500	—	kHz	RRT = 200 kΩ *1
Zero current detector	ZCD threshold voltage	Vzcd	1	3	6	mV	
	Input bias current	Ics	–58	–42	–25	μA	Vcs = 0 V
	CS open detect threshold voltage	Vcs-open	45	72.5	130	mV	
Restart	Restart time delay	Tstart	75	150	330	μs	FB = 2.0 V COMP = 2.5 V

Notes: *1 Design spec

*2 dVramp = Vclamp_comp – Voff_ramp

Electrical Characteristics (cont.)

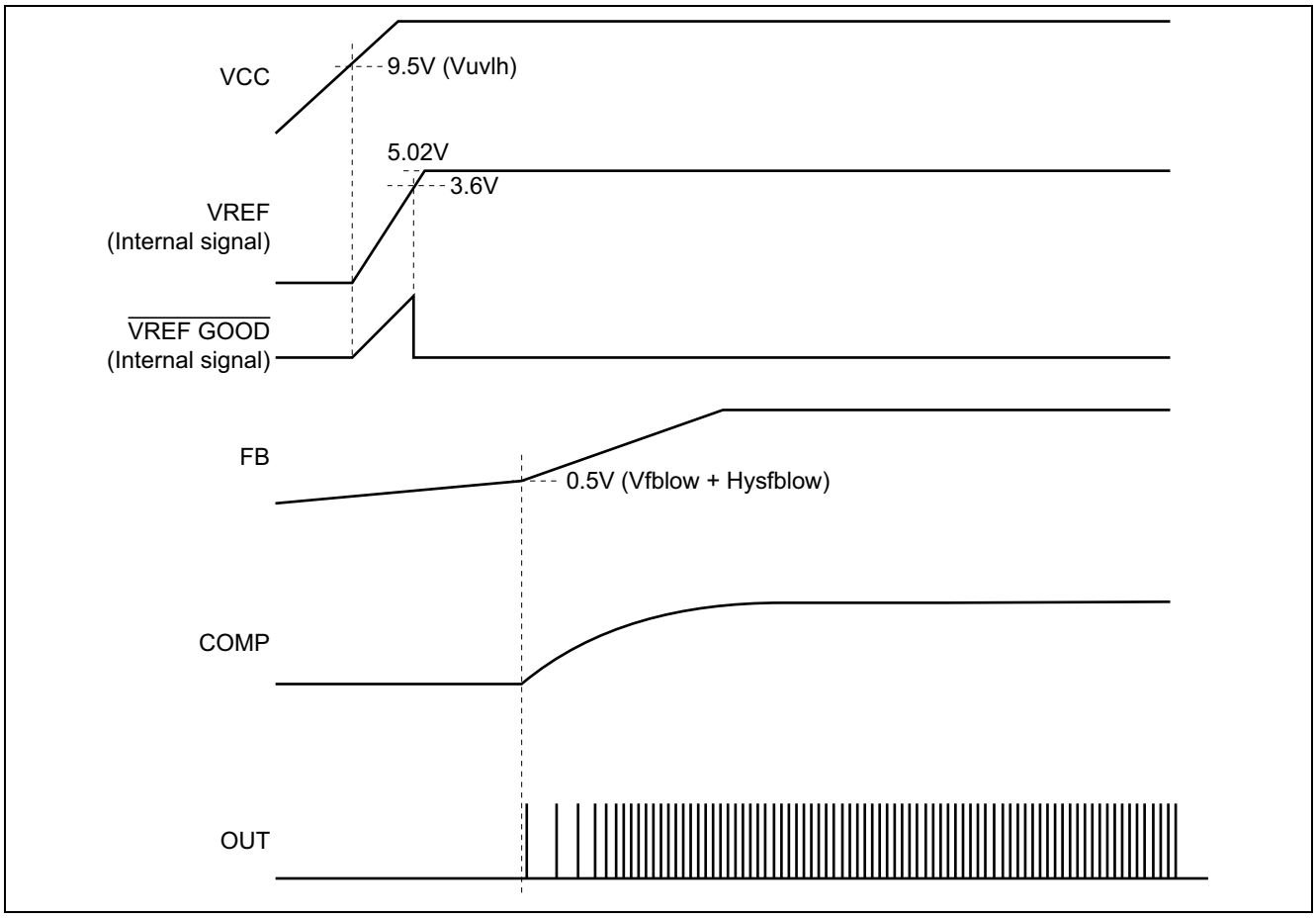
(Ta = 25°C, VCC = 12 V, CS = 0.04 V, FB = 2 V, COMP: Open, OVP2 = 1 V, RRT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Out	Rise time	tr-out	—	35	100	ns	CL = 1000 pF 
	Fall time	tf-out	—	35	100	ns	CL = 1000 pF 
	Out low voltage	Vol1-out	—	0.08	0.2	V	Isink = 20 mA
		Vol2-out	—	0.05	0.7	V	VCC = 5 V, Isink = 10 mA
	Out high voltage	Voh-out	11.5	11.8	—	V	Isource = –20 mA
Over current protection	OCP threshold voltage	Vocp	–0.63	–0.6	–0.57	V	
Over & Under voltage protection	Dynamic OVP threshold voltage	Vdovp	—	Vfb× 1.040	—	V	Measure FB *1
	Dynamic UVP threshold voltage	Vduvp	—	Vfb× 0.920	—	V	*1
	Static OVP threshold voltage	Vsovp	Vfb× 1.075	Vfb× 1.090	Vfb× 1.105	V	
	Static OVP hysteresis	Hys-sovp	50	100	150	mV	
	FB low detect threshold voltage	Vfblow	0.25	0.3	0.35	V	
	FB low detect hysteresis	Hysfblow	0.16	0.20	0.24	V	
	OVP2 high threshold voltage	Vovp2-high	Vfb× 1.18	Vfb× 1.20	Vfb× 1.22	V	Measure OVP2
	OVP2 low threshold voltage	Vovp2-low	0.1	0.2	0.3	V	
	OVP2 source current	Isrc-ovp2	–0.40	–0.15	–0.05	μA	

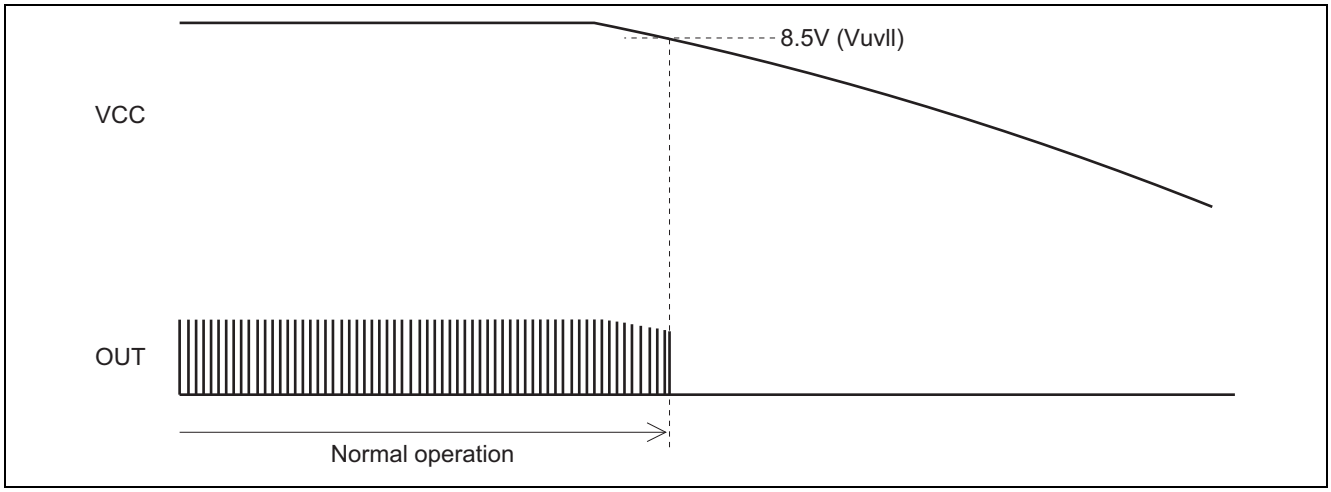
Note: *1 Design spec

Waveforms

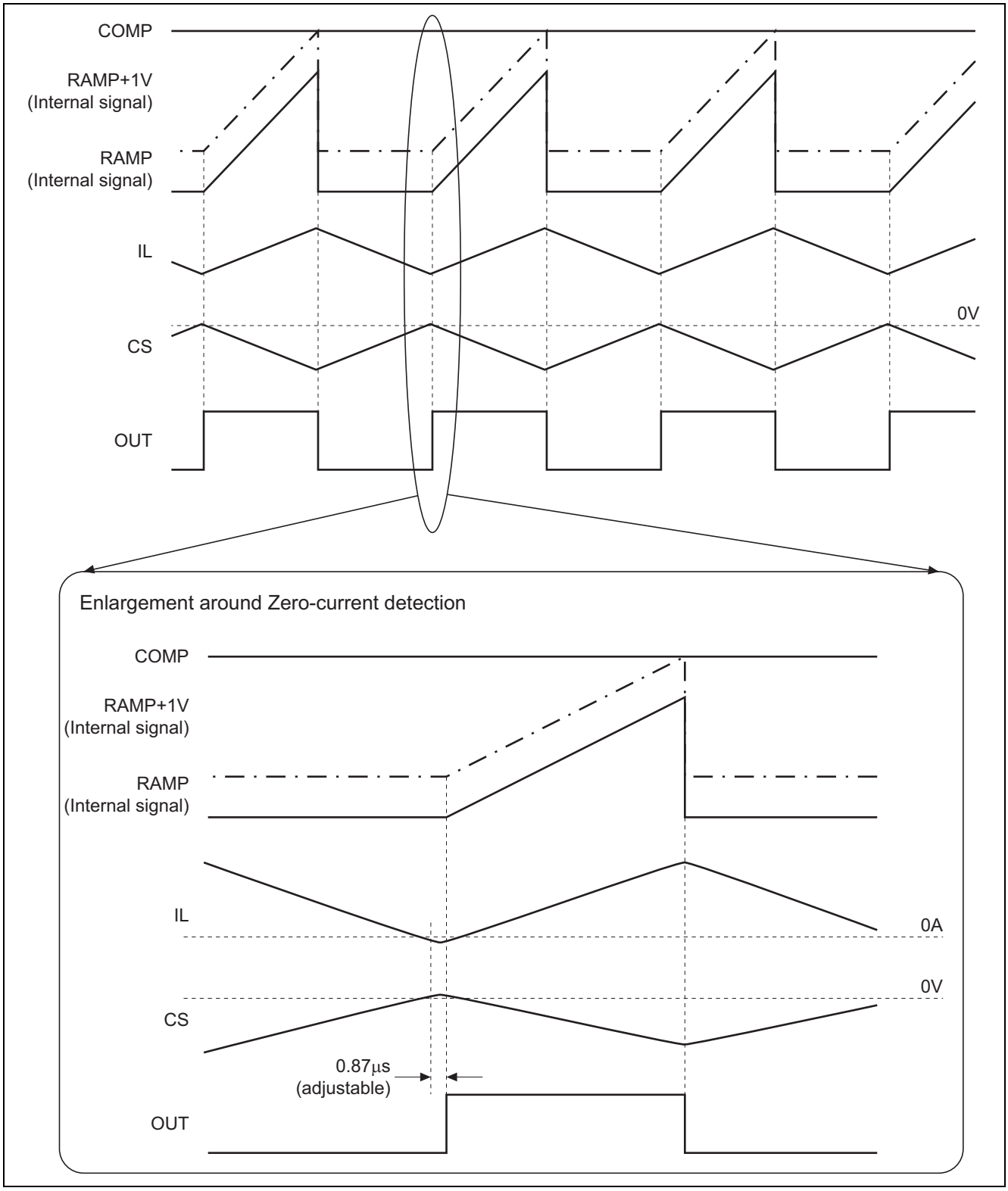
1. Start-up



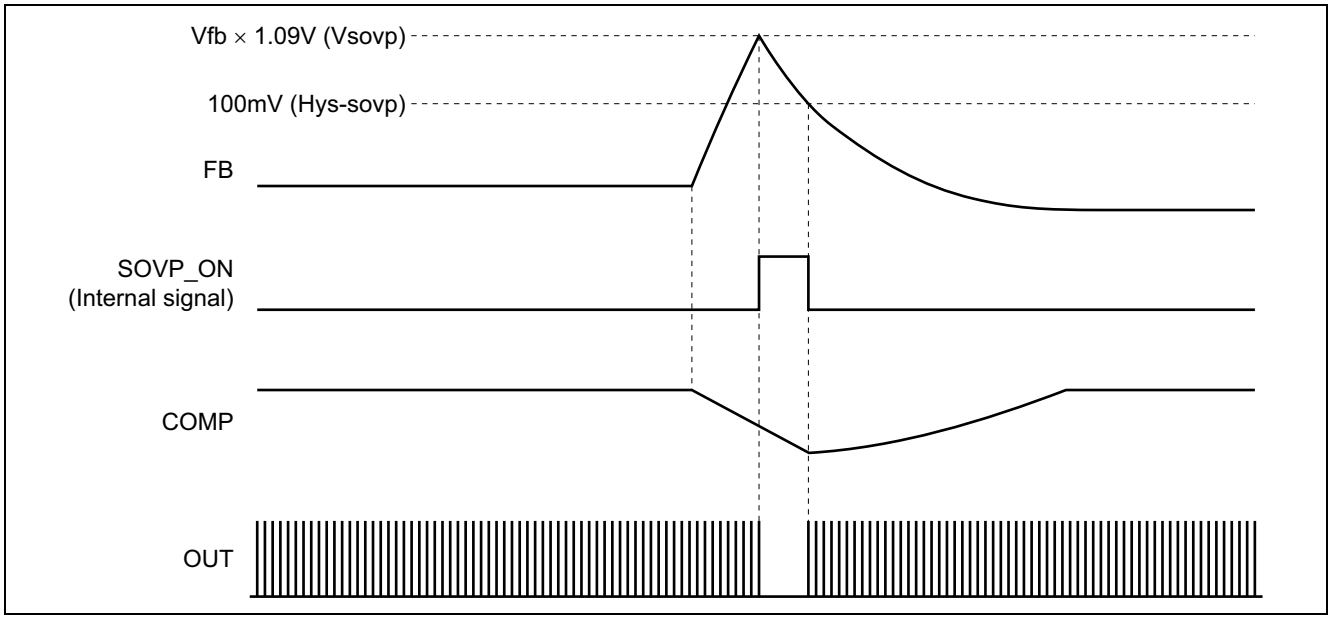
2. Shut-down



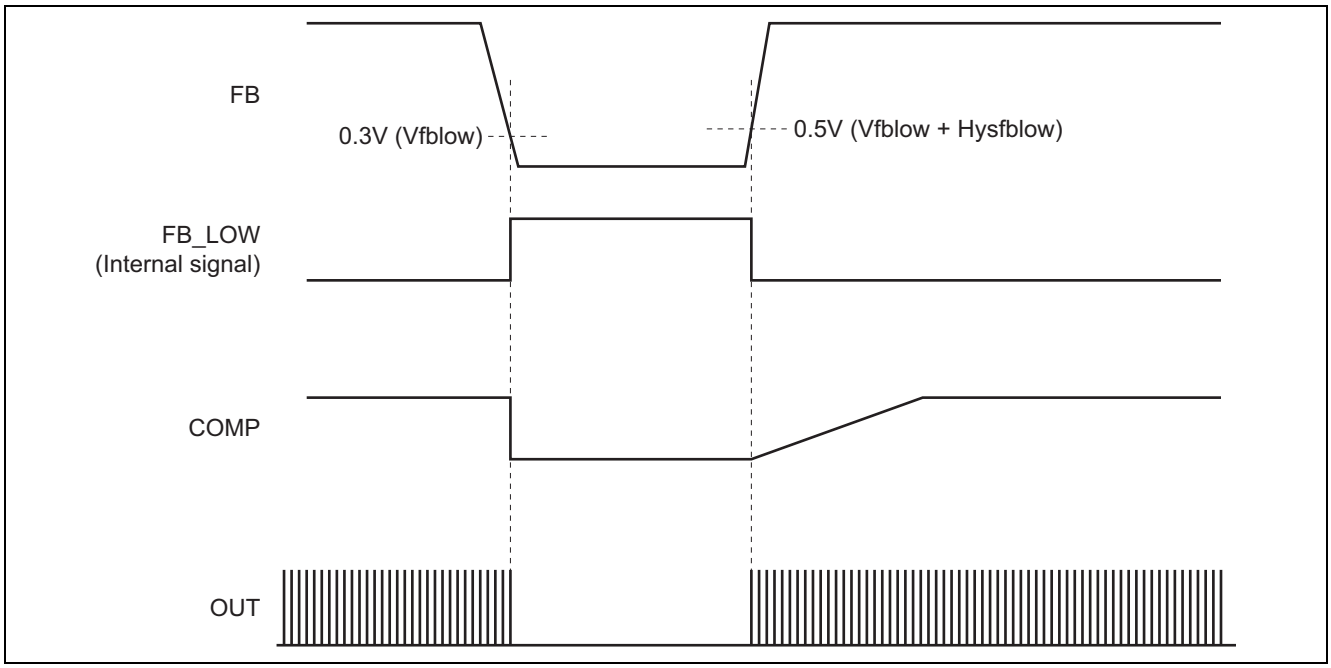
3. Gate Drive Output



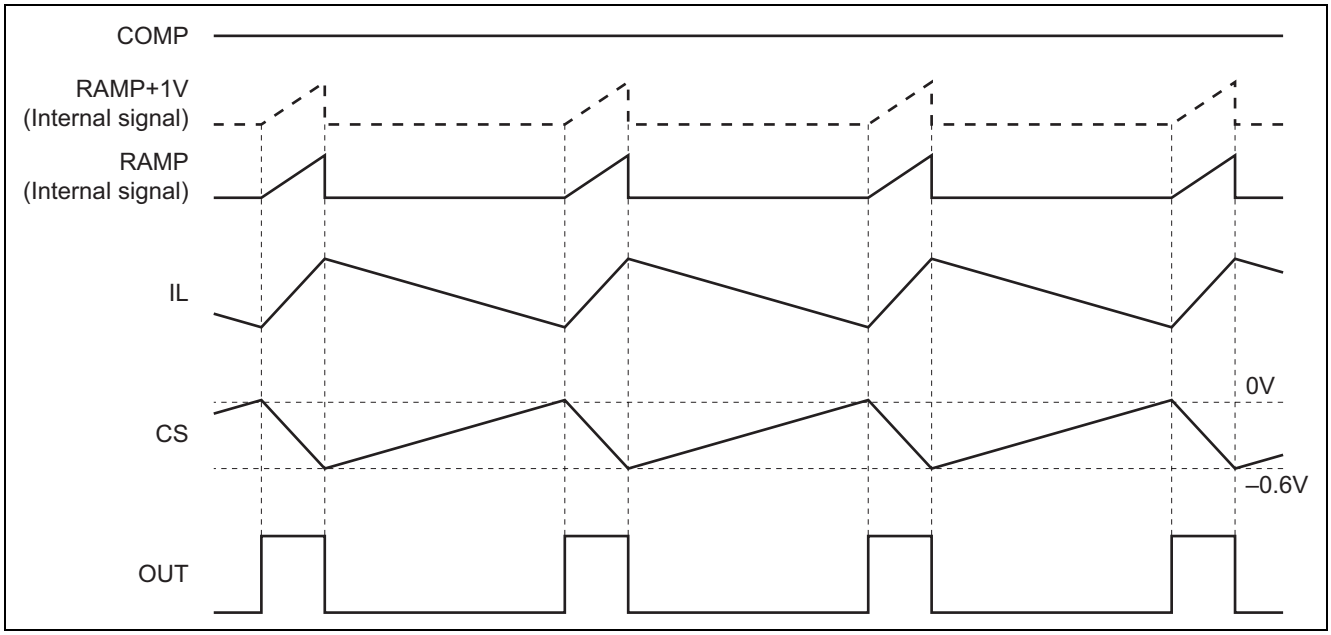
4. Overvoltage Protection (SOVP)



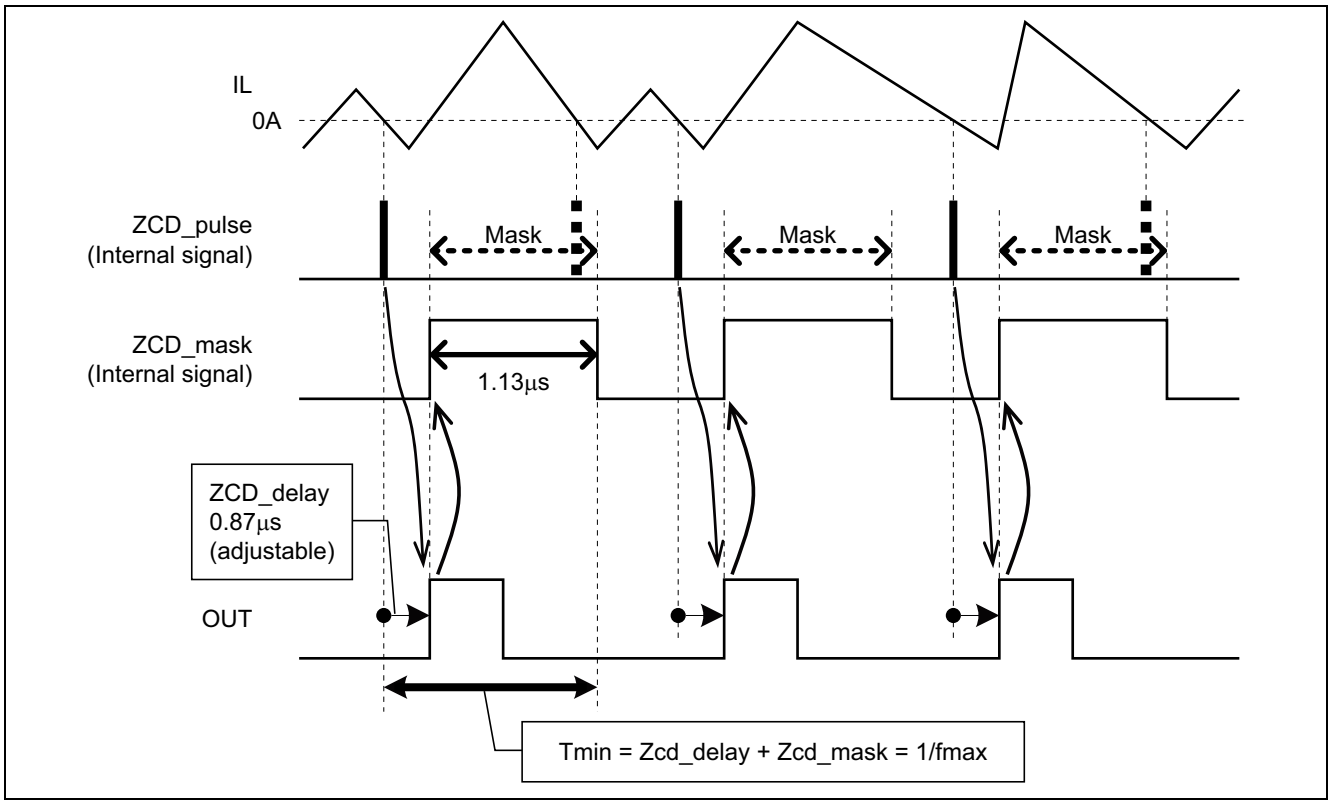
5. FB Low Detection



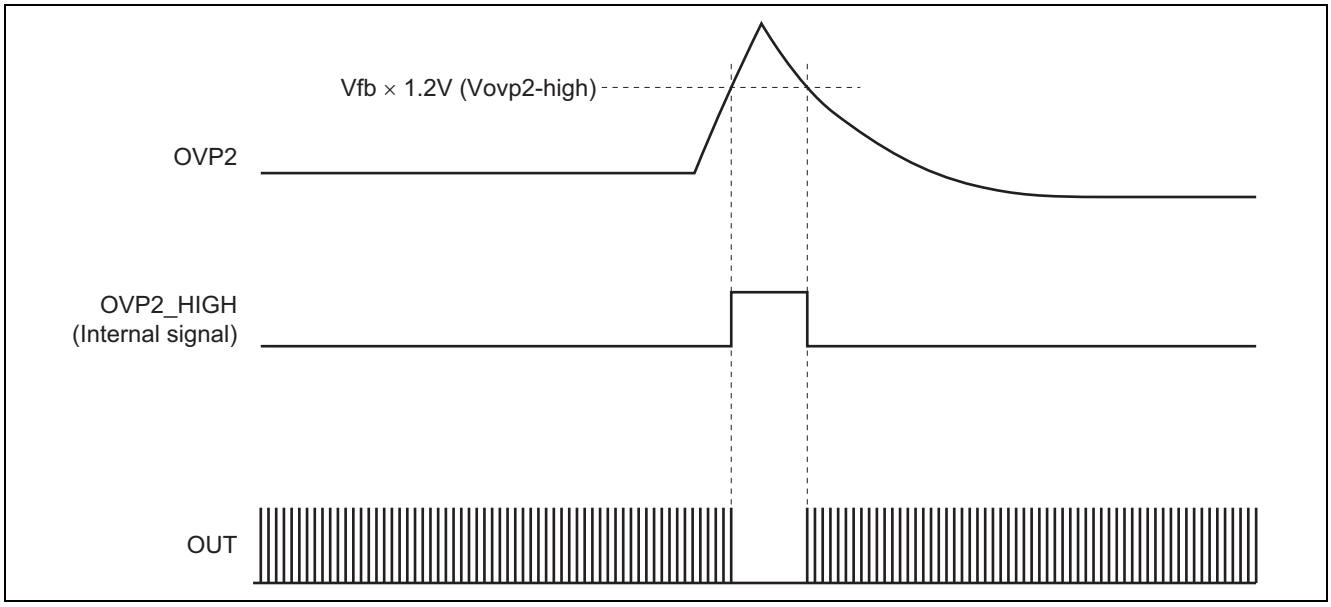
6. Overcurrent Protection (OCP)



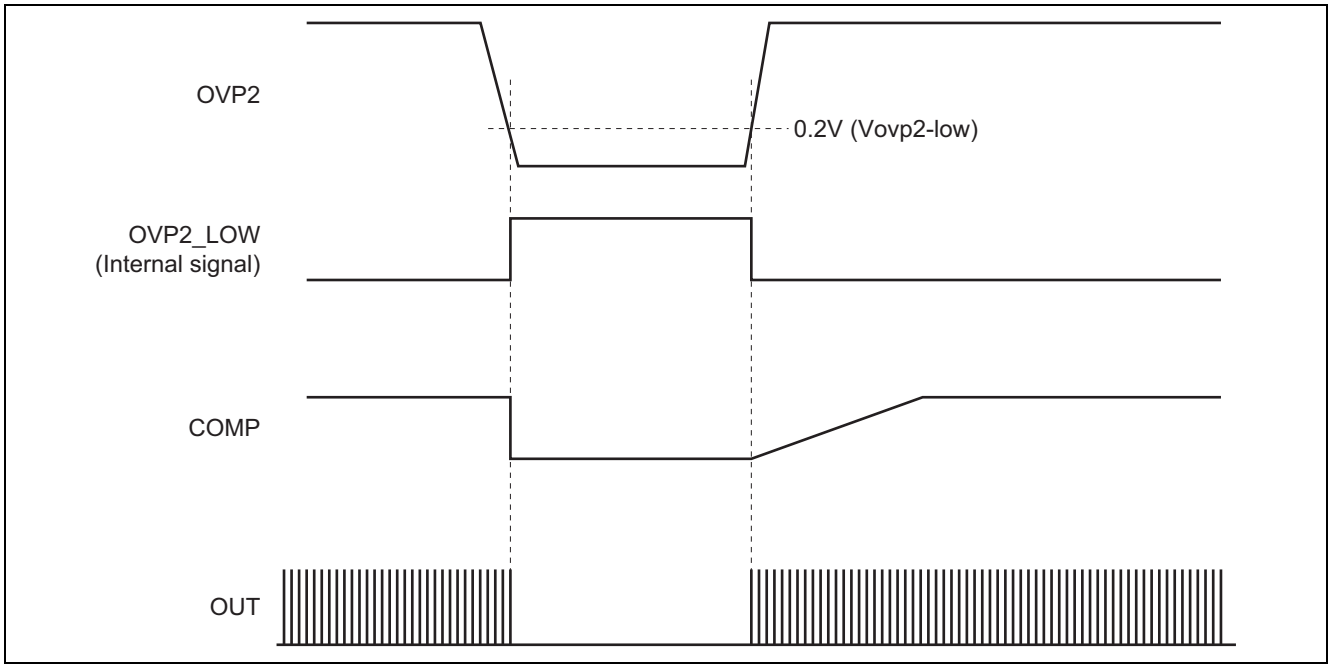
7. Frequency Limiter



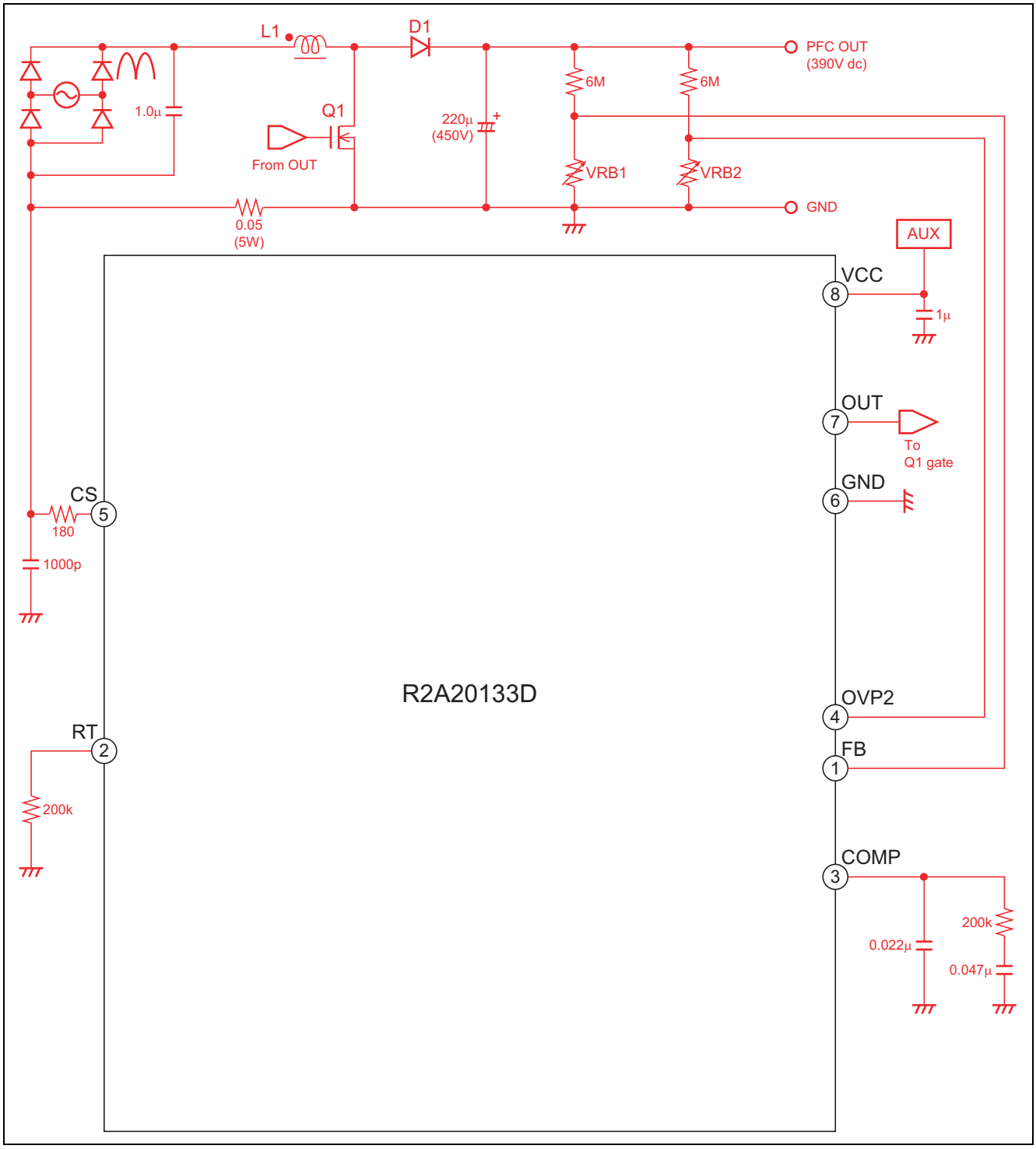
8. Overvoltage Protection 2 (OVP2)



9. OVP2 Low Detection

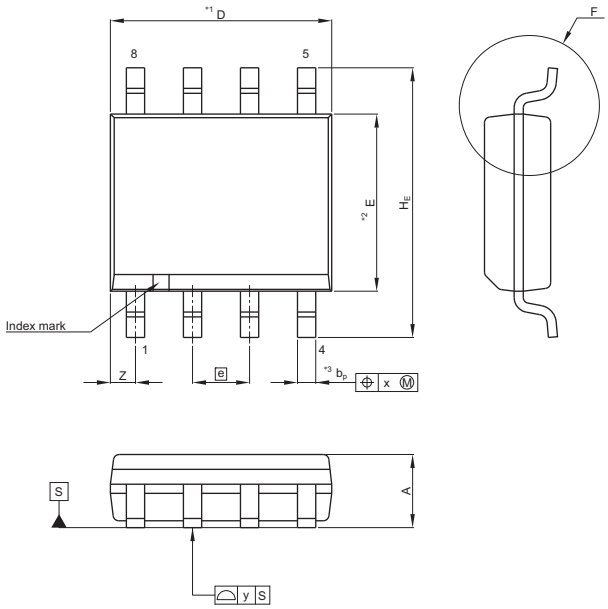


System Diagram

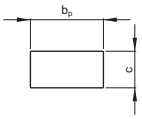


Package Dimensions

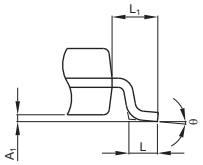
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-3.94x4.93-1.27	PRSP0008DJ-A	—	0.073g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.80	4.93	4.98
E	3.81	3.94	3.99
A_2	—	1.47	—
A_1	0.10	0.15	0.25
A	—	—	1.73
b_p	0.35	0.41	0.49
b_1	—	—	—
c	0.19	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.84	5.99	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
Z	—	0.56	—
L	0.41	0.64	0.89
L_1	—	1.03	—

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