30V N-Channel Enhancement Mode MOSFET

V_{DS}=30V

$R_{DS(ON)}$, Vgs@10V,Ids@30A ≦ 6.6mΩ

$R_{DS(ON)}$, Vgs@4.5V,Ids@15A ≦ 11mΩ

FEATURES

Advanced trench process technology

High density cell design for ultra low on-resistance

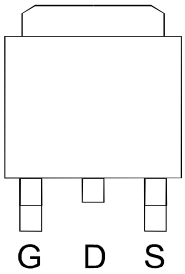
Specially designed for Low-side switching of PWM application.

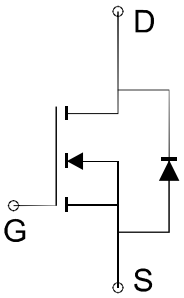
APPLICATIONS

- Motherboard (V-Core)
- Portable Equipment
- DC/DC Converter
- Load Switch
- LCD Display inverter
- IPC

PIN CONFIGURATION (TO-252)

Top View





Ordering Information: ME70N03S (Pb-free)

ME70N03S-G (Green product)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current (Tj=150℃)*	T_C=25℃	I_D	62		A
	T_C=70℃		50		
	T_A=25℃		17		
	T_A=70℃		13		
Pulsed Drain Current		I_{DM}	100		A
Maximum Power Dissipation	T_C=25℃	P_D	41		W
	T_C=70℃		26		
	T_A=25℃		3.1		
	T_A=70℃		2		
Operating Junction and Storage Temperature Range		T_J, Tstg	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	15	℃/W
			Steady State	40	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	3		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

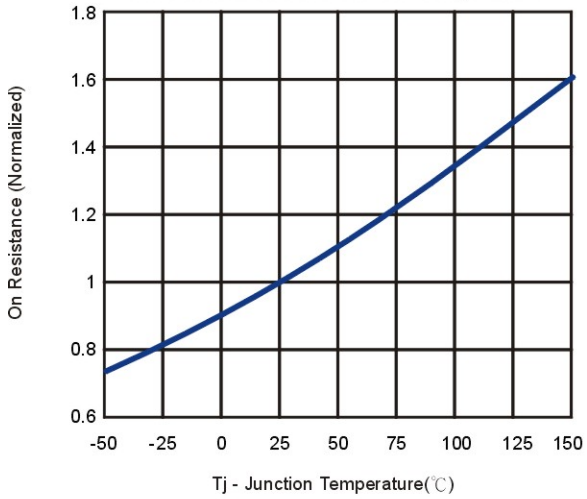
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=30A		5.5	6.6	mΩ
		V_{GS}=4.5V, I_D=15A		8.5	11	
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=25A		38		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=25A		19.5		
Qgs	Gate-Source Charge			8		
Qgd	Gate-Drain Charge			11		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, F=1MHz		1620		pF
Coss	Output Capacitance			255		
Crss	Reverse Transfer Capacitance			80		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.1		Ω
$t_{d(on)}$	Turn-On Delay Time	R_L=15Ω, V_{GEN} =10V, I_D=1A V_{DD}=15V, R_G=3Ω		17		ns
tr	Turn-On Rise Time			15		
$t_{d(off)}$	Turn-Off Delay Time			58		
tf	Turn-Off Fall Time			6		
SOURCE-DRAIN DIODE						
I_S	Max.Diode Forward Current				20	A
V_{SD}	Diode Forward Voltage	I_S=20A, V_{GS}=0V		0.85	1.2	V

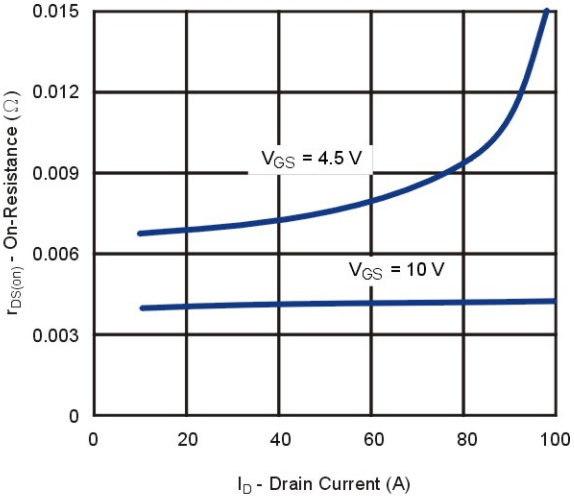
Note: a.Pulse test: pulse width＜=300us, duty cycle＜=2%

Typical Characteristics (T_J =25℃ Noted)

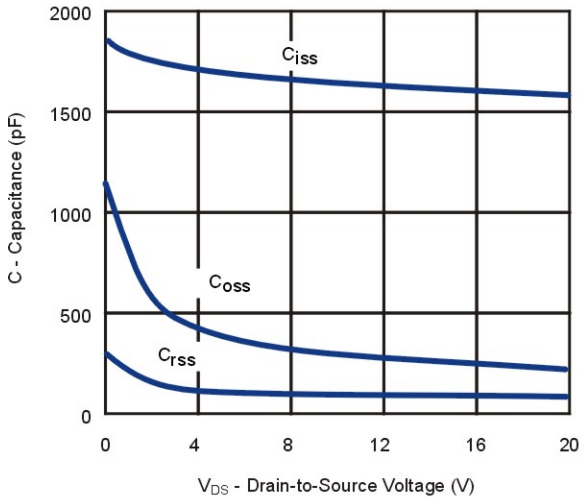
On Resistance vs. Junction Temperature



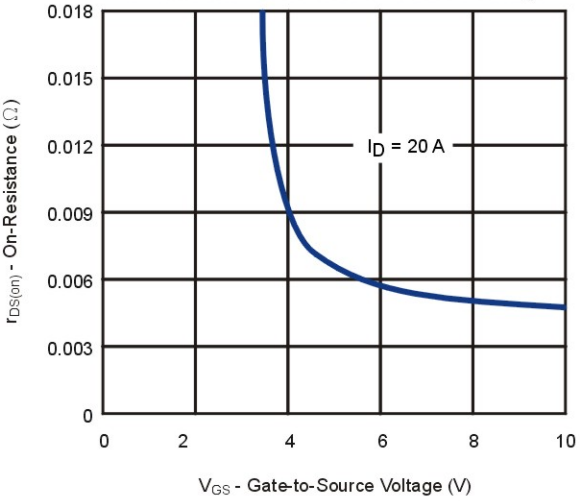
On-Resistance vs. Drain Current



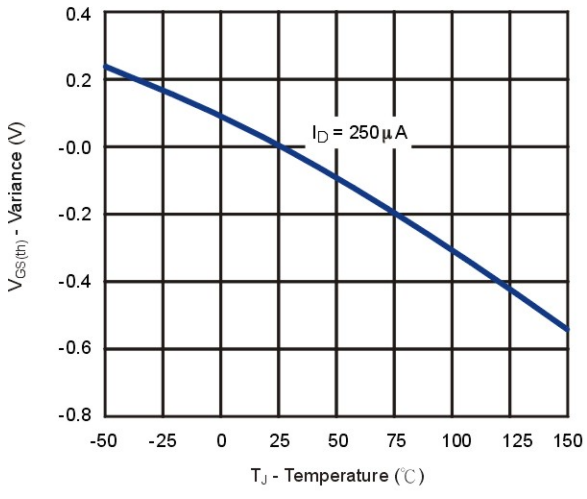
Capacitance



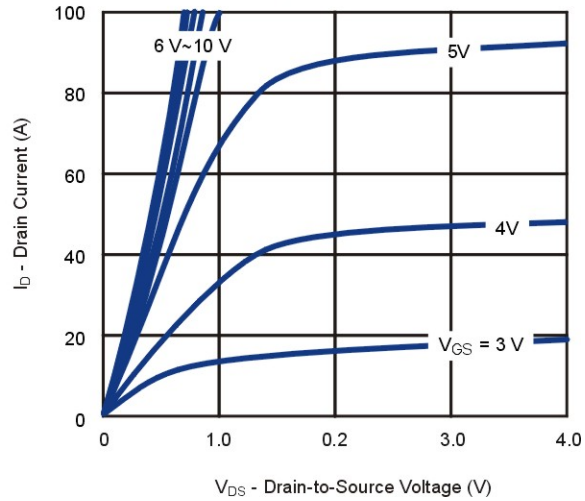
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

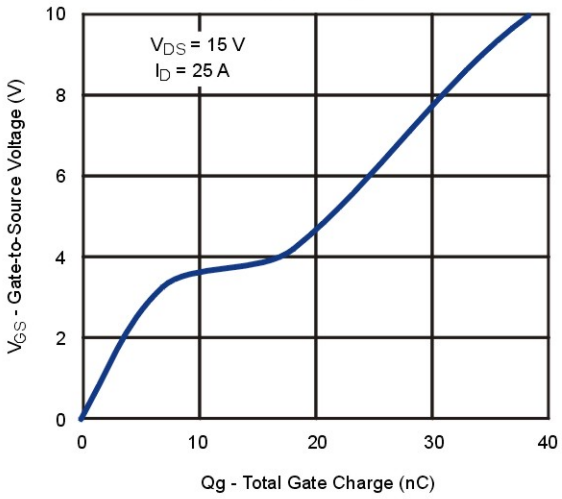


On-Region Characteristics

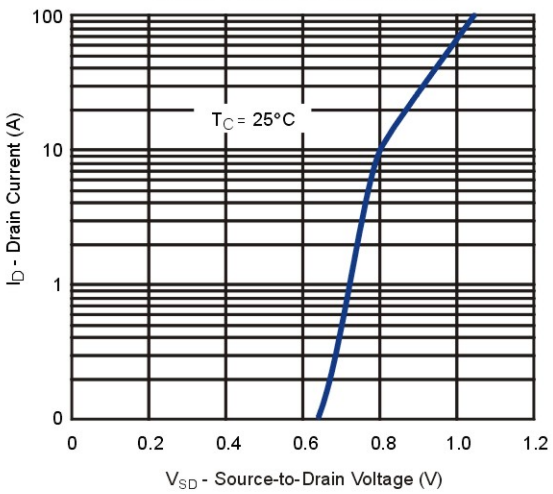


Typical Characteristics (T_J =25℃ Noted)

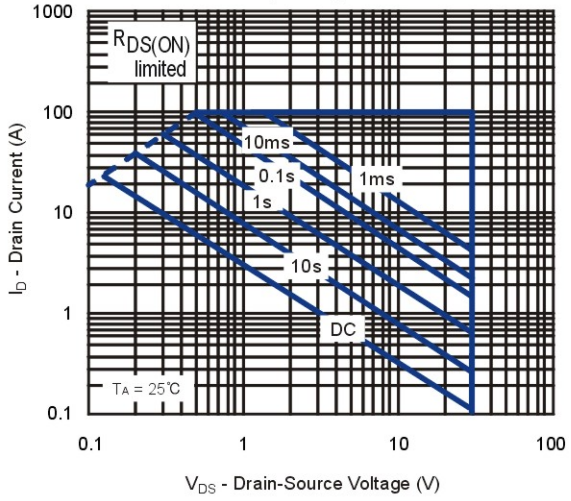
Gate Charge



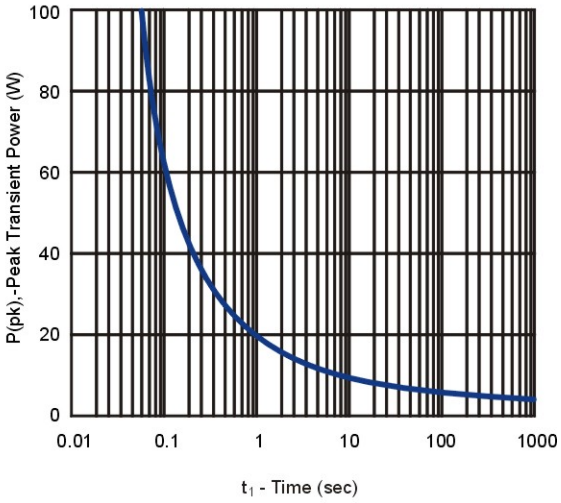
On-Resistance vs. Drain Current



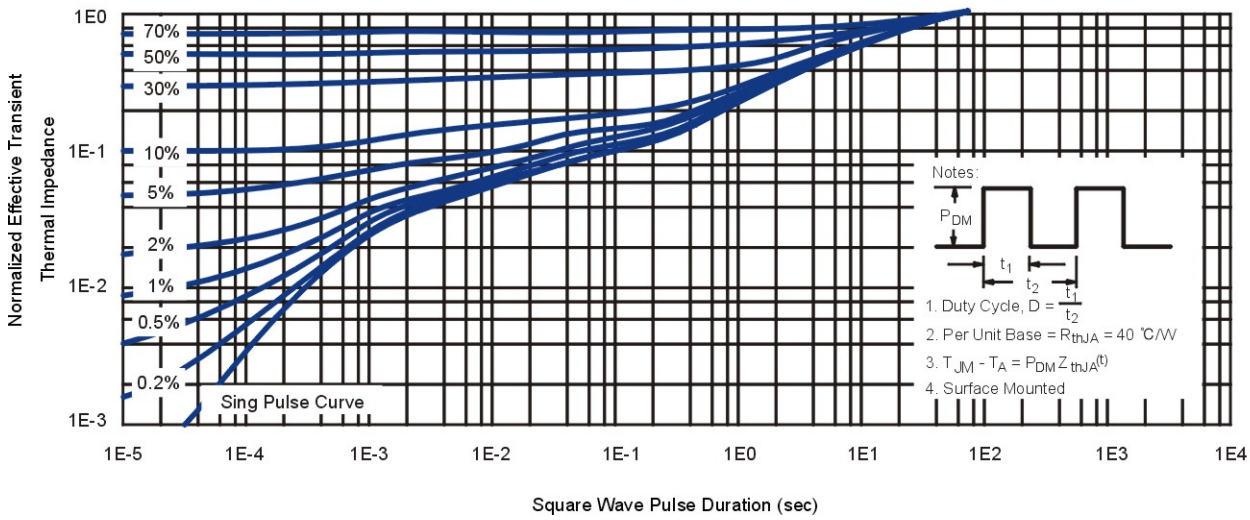
Maximum Forward Biased Safe Operating Area



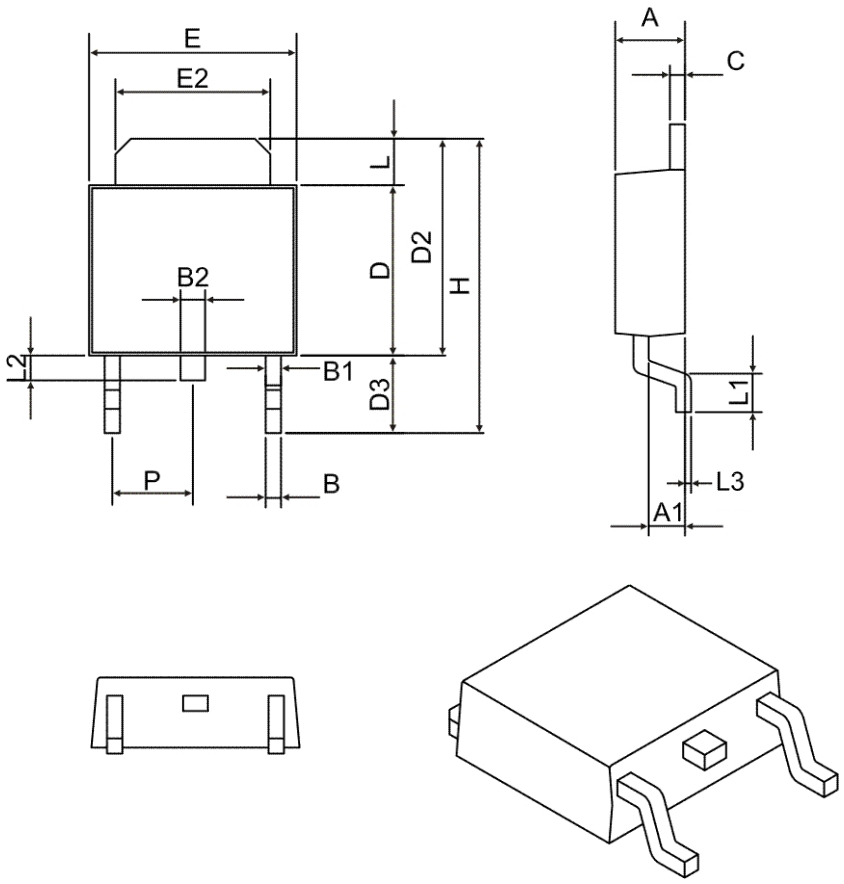
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



TO-252 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.00	2.50
A1	0.90	1.30
B	0.50	0.85
B1	0.50	0.80
B2	0.50	1.00
C	0.40	0.60
D	5.20	5.70
D2	6.50	7.30
D3	2.20	3.00
H	9.50	10.50
E	6.30	6.80
E2	4.50	5.50
L	1.30	1.70
L1	0.90	1.70
L2	0.50	1.10
L3	0	0.30
P	2.00	2.80