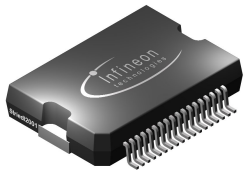
# Smart 16-fold Low-Side Switch

## Features

- Short Circuit Protection
- Overtemperature Protection
- Overvoltage Protection
- 16 bit Serial Data Input and Diagnostic Output (2 bit/chan. acc. SPI Protocol)
- Direct Parallel Control of Eight channels for PWM Applications
- Parallel Inputs High or Low Active Programmable
- General Fault Flag
- Low Quiescent Current
- Compatible with 3V Microcontrollers
- **E**lecto**s**tatic **d**ischarge (ESD) Protection

## Product Summary

| | | | |
|---|---|---|---|
| Supply voltage | $V_S$ | 4.5 – 5.5 | V |
| Drain source clamping voltage | $V_{DS(AZ)max}$ | 60 | V |
| On resistance | $R_{ON\ 1\text{-}8}$ | 1.0 | Ω |
| | $R_{ON\ 10,11,14,15}$ | 0.35 | Ω |
| | $R_{ON\ 9,12,13,16}$ | 0.3 | Ω |
| Output current (Channel 1-8) | $I_{D(NOM)}$ | 0.5 | A |
| (Channel 9-16) | $I_{D(NOM)}$ | 1 | A |



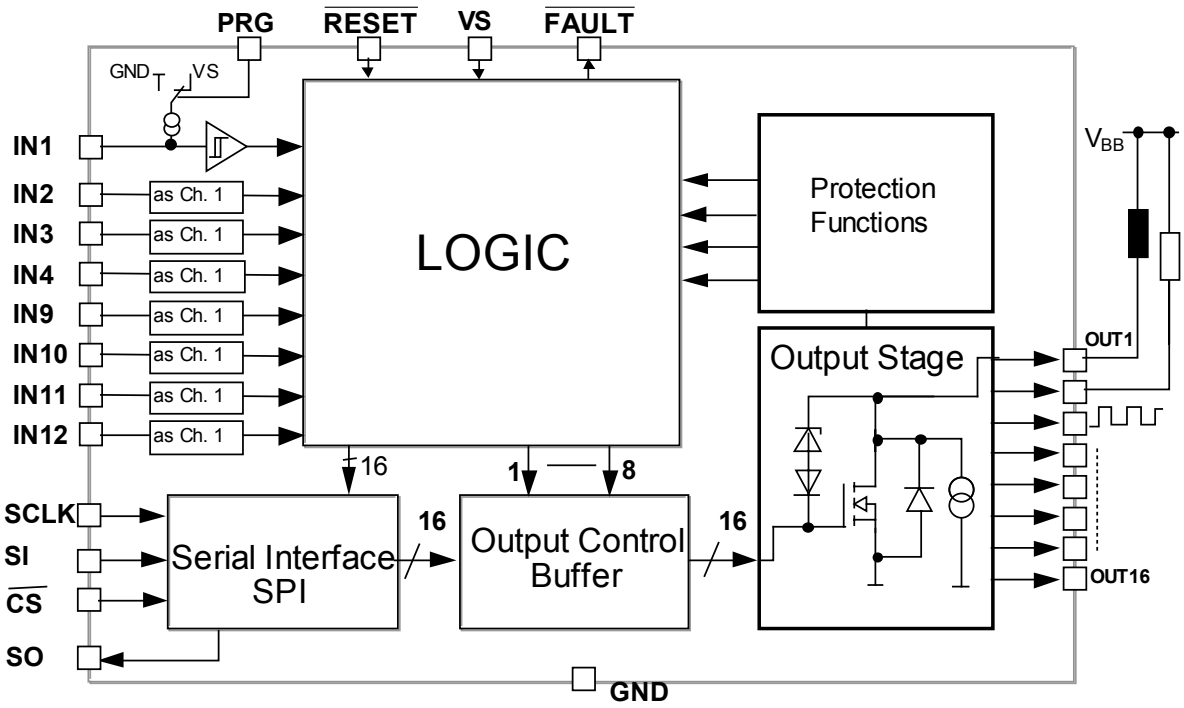
**P-DSO 36-12**
Ordering Code:
Q67007-A9470

## Application

- µC Compatible Power Switch for 12 V and 24 V Applications
- Switch for Automotive and Industrial System
- Solenoids, Relays and Resistive Loads
- Robotic Controls

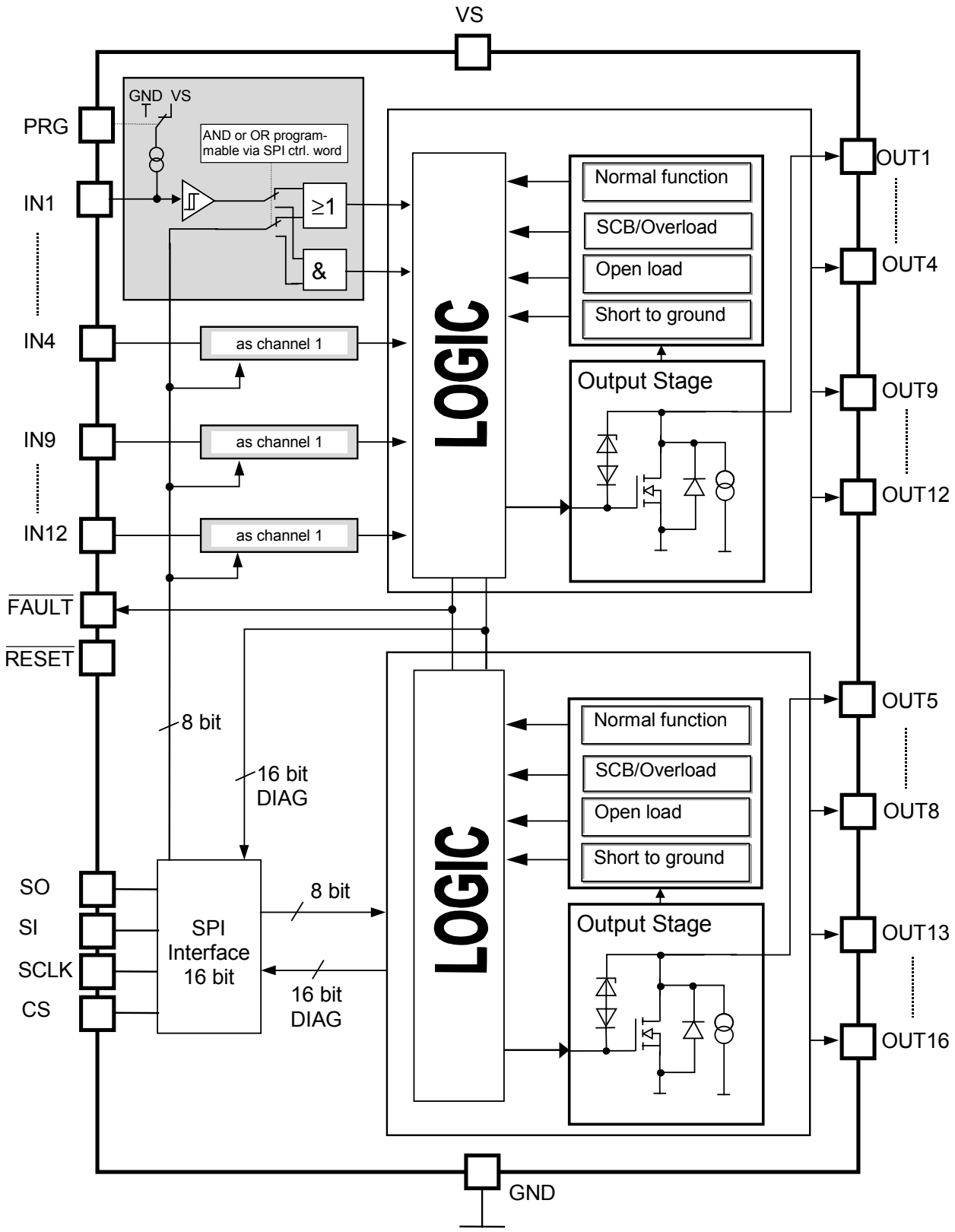
## General description

16-fold Low-Side Switch (8 x 1.3 Ω, 4 x 0.4 Ω, 4 x 0.35 Ω) in Smart Power Technology (SPT) with a **S**erial **P**eripheral **I**nterface (SPI) and 16 open drain DMOS output stages. The TLE 6240 GP is protected by embedded protection functions and designed for automotive and industrial applications. The output stages are controlled via SPI Interface. Additionally 8 channels can be controlled direct in parallel for PWM applications. Therefore the TLE 6240 GP is particularly suitable for engine management and powertrain systems, safety and body applications.



## Detailed Block Diagram

All 16 channels can be controlled via the serial interface (SPI). In addition to the serial control it is possible to con-



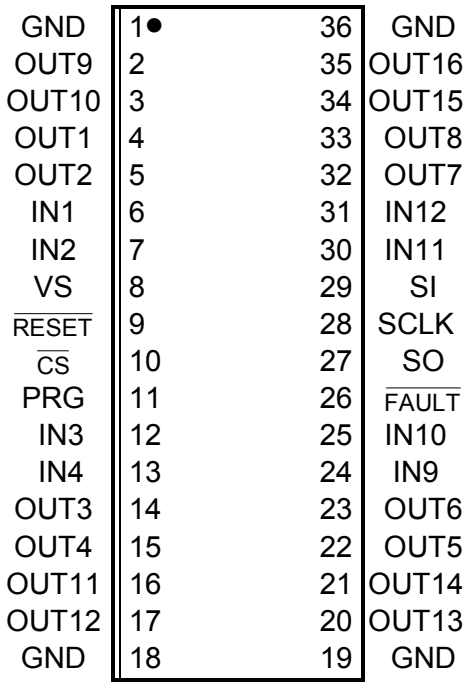

trol channel 1 to 4 and 9 to 12 direct in parallel with a separate input pin. The parallel input signal is either ORed or ANDed with the respective SPI data bit. This boolean operation can be programmed via SPI control byte (see chapter "Functional Description"). The SPI interface also performs a diagnostic information for each channel.

## Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | OUT9 | Power Output Channel 9 |
| 3 | OUT10 | Power Output Channel 10 |
| 4 | OUT1 | Power Output Channel 1 |
| 5 | OUT2 | Power Output Channel 2 |
| 6 | IN1 | Input Channel 1 |
| 7 | IN2 | Input Channel 2 |
| 8 | VS | Supply Voltage |
| 9 | $\overline{\text{RESET}}$ | Reset |
| 10 | $\overline{\text{CS}}$ | Chip Select |
| 11 | PRG | Program (inputs high or low-active) |
| 12 | IN3 | Input Channel 3 |
| 13 | IN4 | Input Channel 4 |
| 14 | OUT3 | Power Output Channel 3 |
| 15 | OUT4 | Power Output Channel 4 |
| 16 | OUT11 | Power Output Channel 11 |
| 17 | OUT12 | Power Output Channel 12 |
| 18 | GND | Ground |
| 19 | GND | Ground |
| 20 | OUT13 | Power Output Channel 13 |
| 21 | OUT14 | Power Output Channel 14 |
| 22 | OUT5 | Power Output Channel 5 |
| 23 | OUT6 | Power Output Channel 6 |
| 24 | IN9 | Input Channel 9 |
| 25 | IN10 | Input Channel 10 |
| 26 | $\overline{\text{FAULT}}$ | General Fault Flag |
| 27 | SO | Serial Data Output |
| 28 | SCLK | Serial Clock |
| 29 | SI | Serial Data Input |
| 30 | IN11 | Input Channel 11 |
| 31 | IN12 | Input Channel 12 |
| 32 | OUT7 | Power Output Channel 7 |
| 33 | OUT8 | Power Output Channel 8 |
| 34 | OUT15 | Power Output Channel 15 |
| 35 | OUT16 | Power Output Channel 16 |
| 36 | GND | Ground |

Heat Slug internally connected to ground pins

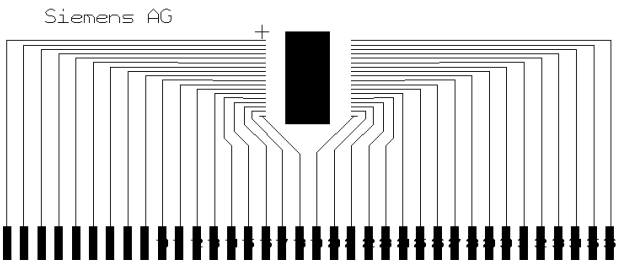
## Pin Configuration (Top view)



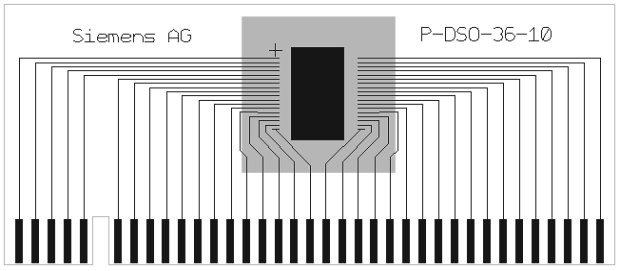

Power SO 36

## Maximum Ratings for $T_j$ = – 40°C to 150°C

| Parameter | Symbol | Values | Unit |
|---|---|---|---|
| Supply Voltage | $V_S$ | -0.3 ... +7 | V |
| Continuous Drain Source Voltage (OUT1...OUT16) | $V_{DS}$ | 45 | V |
| Input Voltage, All Inputs and Data Lines | $V_{IN}$ | - 0.3 ... + 7 | V |
| Load Dump Protection $V_{Load\ Dump}$ = $U_P$+$U_S$; $U_P$=13.5 V<br>$R_I$[1]=2 Ω; $t_d$=400ms; IN = low or high<br>Channel 1-8 with Automotive Relay $R_L$ = 65 Ω<br>Channel 9-16 with Automotive Injector Valve $R_L$ = 14 Ω<br>$R_I$=2 Ω; $t_d$=400ms; IN = low or high<br>Channel 1-8 with Load $R_L$ = 24 Ω<br>Channel 9-16 with Load $R_L$ = 6.8 Ω | $V_{Load\ Dump}$[2] | <br><br>90<br>65<br><br>65<br>50 | V |
| Output Current per Channel (see el. characteristics) | $I_{D(lim)}$ | $I_{D(lim)\ min}$ | A |
| Output Current per Channel @ $T_A$ = 25°C<br>(All 16 Channels ON; Mounted on PCB )[3] | $I_{D1-8}$<br>$I_{D9-16}$ | 0.3<br>0.5 | A |
| Output Current<br>(Max. total current of all channels on; Heat Sink required) | $I_{Dmax}$ | 14 | A |
| Single Pulse Inductive Energy (internal clamping)<br>$T_J$ = 25°C, $I_{D1-8}$ = 0.5 A, $I_{D9-16}$ = 1 A | $E_{AS}$ | 50 | mJ |
| Power Dissipation (DC, mounted on PCB) @ $T_A$ = 25°C | $P_{tot}$ | 3.3 | W |
| **E**lectro**s**tatic **D**ischarge **V**oltage (Human Body Model)<br>according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993 | $V_{ESD}$ | 2000 | V |
| DIN Humidity Category, DIN 40 040 | | E | |
| IEC Climatic Category, DIN IEC 68-1 | | 40/150/56 | |
| Thermal Resistance<br>junction - case (die soldered on heat slug)<br>junction - ambient @ min. footprint<br>junction - ambient @ 6 cm$^2$ cooling area with heat pipes | <br>$R_{thJC}$<br>$R_{thJA}$<br> | <br>1.5<br>50<br>38 | <br>K/W<br><br> |




Minimum footprint




PCB with heat pipes,
back side 6 cm$^2$ cooling area

[1] $R_I$=internal resistance of the load dump test pulse generator LD200
[2] $V_{LoadDump}$ is setup without DUT connected to the generator per ISO 7637-1 and DIN 40 839.
[3] Output current rating so long as maximum junction temperature is not exceeded. At $T_A$ = 125 °C the output current has to be calculated using $R_{thJA}$ according mounting conditions.

## Electrical Characteristics

| Parameter and Conditions<br>$V_S$ = 4.5 to 5.5 V ; $T_j$ = - 40 °C to + 150 °C; Reset = H<br>(unless otherwise specified) | | Symbol | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **1. Power Supply, Reset** | | | | | | |
| Supply Voltage[4] | | $V_S$ | 4.5 | -- | 5.5 | V |
| Supply Current | | $I_S$ | -- | 5 | 10 | mA |
| Supply Current in Standby Mode (RESET = L) | | $I_{S(stdy)}$ | -- | 10 | 50 | µA |
| Minimum Reset Duration<br>(After a reset all parallel inputs are ORed with the SPI data bits) | | $t_{Reset,min}$ | 10 | -- | -- | µs |
| **2. Power Outputs** | | | | | | |
| ON Resistance $V_S$ = 5 V<br>Channel 1 ... 8 | $T_J$ = 25°C<br>$T_J$ = 150°C | $R_{DS(ON)}$ | --<br>-- | 1<br>1.7 | 1.3<br>2.2 | Ω |
| ON Resistance $V_S$ = 5 V<br>Channel 10, 11, 14, 15 | $T_J$ = 25°C<br>$T_J$ = 150°C | $R_{DS(ON)}$ | --<br>-- | 0.35<br>0.60 | 0.40<br>0.70 | Ω |
| ON Resistance $V_S$ = 5 V<br>Channel 9, 12, 13, 16 | $T_J$ = 25°C<br>$T_J$ = 150°C | $R_{DS(ON)}$ | --<br>-- | 0.30<br>0.50 | 0.35<br>0.60 | Ω |
| Output Clamping Voltage<br>Output OFF | Channel 1-8<br>Channel 9-16 | $V_{DS(AZ)}$ | 45<br>45 | 50<br>52,5 | 60<br>60 | V |
| Current Limit | Channel 1...8<br>Channel 9...16 | $I_{D(lim)}$ | 1<br>3 | 1.5<br>4.5 | 2<br>6 | A |
| Output Leakage Current | $V_{Reset}$ = L | $I_{D(lkg)}$ | -- | -- | 10 | µA |
| Turn-On Time | $I_D$ = 0.5 A, resistive load | $t_{ON}$ | -- | 6 | 12 | µs |
| Turn-Off Time | $I_D$ = 0.5 A, resistive load | $t_{OFF}$ | -- | 6 | 12 | µs |
| **3. Digital Inputs** | | | | | | |
| Input Low Voltage | | $V_{INL}$ | - 0.3 | -- | 1.0 | V |
| Input High Voltage | | $V_{INH}$ | 2.0 | -- | -- | V |
| Input Voltage Hysteresis | | $V_{INHys}$ | 50 | 100 | 200 | mV |
| Input Pull Down/Up Current (IN1...4, IN9...12) | $V_{IN}$ = 5 V | $I_{IN(1..4,9...12)}$ | 20 | 50 | 100 | µA |
| PRG, Reset Pull Up Current | | $I_{IN(PRG,Res)}$ | 20 | 50 | 100 | µA |
| Input Pull Down Current (SI, SCLK) | | $I_{IN(SI,SCLK)}$ | 10 | 20 | 50 | µA |
| Input Pull Up Current ( $\overline{CS}$ ) | | $I_{IN(CS)}$ | 10 | 20 | 50 | µA |
| **4. Digital Outputs (SO, $\overline{FAULT}$ )** | | | | | | |
| SO High State Output Voltage | $I_{SOH}$ = 2 mA | $V_{SOH}$ | $V_S$ - 0.4 | -- | -- | V |
| SO Low State Output Voltage | $I_{SOL}$ = 2.5 mA | $V_{SOL}$ | -- | -- | 0.4 | V |
| Output Tri-state Leakage Current | $\overline{CS}$ = H, 0 ≤ $V_{SO}$ ≤ $V_S$ | $I_{SOlkg}$ | -10 | 0 | 10 | µA |
| FAULT Output Low Voltage | $I_{FAULT}$ = 1.6 mA | $V_{FAULTL}$ | -- | -- | 0.4 | V |

[4] For $V_S$ < 4.5V the power stages are switched according the input signals and data bits or are definitely switched off. This undervoltage reset gets active at $V_S$ = 3V (typ. value) and is guaranteed by design.

## Electrical Characteristics cont.

| Parameter and Conditions<br>$V_S$ = 4.5 to 5.5 V ; $T_j$ = - 40 °C to + 150 °C ; Reset = H<br>(unless otherwise specified) | | Symbol | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **5. Diagnostic Functions** | | | | | | |
| Open Load Detection Voltage | | $V_{DS(OL)}$ | $V_S$ -2.5 | $V_S$ -2 | $V_S$ -1.3 | V |
| Output Pull Down Current | $V_{Reset}$ = H | $I_{PD(OL)}$ | 50 | 90 | 150 | µA |
| Fault Delay Time | | $t_{d(fault)}$ | 50 | 100 | 200 | µs |
| Short to Ground Detection Voltage | | $V_{DS(SHG)}$ | $V_S$ –3.3 | $V_S$ -2.9 | $V_S$ -2.5 | V |
| Short to Ground Detection Current | $V_{Reset}$ = H | $I_{SHG}$ | -50 | -100 | -150 | µA |
| Overload Detection Threshold | | $I_{D(lim)\ 1...8}$<br>$I_{D(lim)\ 9...16}$ | 1<br>3 | 1.3<br>4 | 2<br>6 | A |
| Overtemperature Shutdown Threshold[5]<br>Hysteresis[5] | | $T_{th(sd)}$<br>$T_{hys}$ | 170<br>-- | --<br>10 | 200<br>-- | °C<br>K |
| **6. SPI-Timing** | | | | | | |
| Serial Clock Frequency (depending on SO load) | | $f_{SCK}$ | DC | -- | 5 | MHz |
| Serial Clock Period (1/fclk) | | $t_{p(SCK)}$ | 200 | -- | -- | ns |
| Serial Clock High Time | | $t_{SCKH}$ | 50 | -- | -- | ns |
| Serial Clock Low Time | | $t_{SCKL}$ | 50 | -- | -- | ns |
| Enable Lead Time (falling edge of $\overline{CS}$ to rising edge of CLK) | | $t_{lead}$ | 200 | -- | -- | ns |
| Enable Lag Time (falling edge of CLK to rising edge of $\overline{CS}$) | | $t_{lag}$ | 200 | --- | -- | ns |
| Data Setup Time (required time SI to falling of CLK) | | $t_{SU}$ | 20 | -- | -- | ns |
| Data Hold Time (falling edge of CLK to SI) | | $t_H$ | 20 | -- | -- | ns |
| Disable Time @ $C_L$ = 50 pF[5] | | $t_{DIS}$ | -- | -- | 150 | ns |
| Transfer Delay Time[6]<br>($\overline{CS}$ high time between two accesses) | | $t_{dt}$ | 200 | -- | -- | ns |
| Data Valid Time | $C_L$ = 50 pF[5]<br>$C_L$ = 100 pF[5]<br>$C_L$ = 220 pF[5] | $t_{valid}$ | --<br>--<br>-- | --<br>--<br>-- | 100<br>120<br>150 | ns |

[5] This parameter will not be tested but guaranteed by design

[6] This time is necessary between two write accesses to control e.g. channel 1 to 8 during the first access and channel 9 to 16 during the second access. To get the correct diagnostic information, the transfer delay time has to be extended to the maximum fault delay time $t_{d(fault)max}$ = 200µs.

# Functional Description

The TLE 6240 GP is an 16-fold low-side power switch which provides a serial peripheral interface (SPI) to control the 16 power DMOS switches, and diagnostic feedback. The power transistors are protected against short to $V_{BB}$, overload, overtemperature and against overvoltage by active zener clamp.
The diagnostic logic recognizes a fault condition which can be read out via the serial diagnostic output (SO).

# Circuit Description

### Power Transistor Protection Functions[7)]

Each of the 16 output stages has its own zener clamp, which causes a voltage limitation at the power transistor when solenoid loads are switched off. The outputs are provided with a current limitation set to a minimum of 1 A for channels 1 to 8 and 3 A for channels 9 to16.
Each output is protected by embedded protection functions. In the event of an overload or short to supply, the current is internally limited and the corresponding bit combination is set (early warning). If this operation leads to an overtemperature condition, a second protection level (about 170 °C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

## SPI Signal Description

**$\overline{\text{CS}}$** - Chip Select. The system microcontroller selects the TLE 6240 GP by means of the $\overline{\text{CS}}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC and vice versa.

**$\overline{\text{CS}}$ High to Low transition:**
- Diagnostic status information is transferred from the power outputs into the shift register.
- Serial input data can be clocked in from then on.
- SO changes from high impedance state to logic high or low state corresponding to the SO bits.

**$\overline{\text{CS}}$ Low to High transition:**
- Transfer of SI bits from shift register into output buffers
.

To avoid any false clocking the serial clock input pin SCLK should be logic low state during high to low transition of $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

**SCLK** - Serial Clock. The system clock pin clocks the internal shift register of the TLE 6240 GP. The serial input (SI) accepts data into the input shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out of the shift register on the

[7)] The integrated protection functions prevent an IC destruction under fault conditions and may not be used in normal operation or permanently

rising edge of serial clock. It is essential that the SCLK pin is in a logic low state whenever chip select $\overline{CS}$ makes any transition.

**SI** - Serial Input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the falling edge of SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.
The input data consist of 16 bit, made up of one control byte and one data byte. The control byte is used to program the device, to operate it in a certain mode as well as providing diagnostic information (see page 14). The eight data bits contain the input information for the eight channels, and are high active.

**SO** - Serial Output. Diagnostic data bits are shifted out serially at this pin, the most significant bit first. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. New diagnostic data will appear at the SO pin following the rising edge of SCLK.

**$\overline{RESET}$** - Reset pin. If the reset pin is in a logic low state, it clears the SPI shift register and switches all outputs OFF. An internal pull-up structure is provided on chip.

## Output Stage Control

The 16 outputs of the TLE 6240 GP can be controlled via serial interface. Additionally eight of these 16 channels can alternatively be controlled in parallel (Channel 1to 4 and 9 to 12) for PWM applications.

### Parallel Control

A Boolean operation (either AND or OR) is performed on each of the parallel inputs and respective SPI data bits, in order to determine the states of the respective outputs. The type of Boolean operation performed is programmed via the serial interface.
The parallel inputs are high or low active depending on the PRG pin. If the parallel input pins are not connected (independent of high or low activity) it is guaranteed that the outputs 1 to 4 and 9 to 12 are switched off. The PRG pin itself is internally pulled up when it is not connected.

| | | |
|---|---|---|
| **PRG** - Program pin. | PRG = High ($V_S$): | Parallel inputs Channel 1to 4 and 9 to 12 are high active |
| | PRG = Low (GND): | Parallel inputs Channel 1 to 4 and 9 to 12 are low active. |

## Serial Control of the Outputs: SPI protocol

Each output is independently controlled by an output latch and a common reset line, which disables all outputs. The Serial Input (SI) is read on the falling edge of the serial clock. A logic high input 'data bit' turns the respective output channel ON, a logic low 'data bit' turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output control buffer.

The 16 channels of the TLE 6240 GP are divided up into two parts for the control of the outputs (ON, OFF) and the diagnosis information.

Channel 1 to 8:

Serial Input (SI) information consists of 16 bit. 8 bit contain the input driver information for channel 1 to 8. The remaining 8 bits are used to program a certain operation mode.
**Control Byte1:** Operation mode and diagnosis select for channels 1 to 8
**Data Byte1:** ON/OFF information for channel 1 to 8

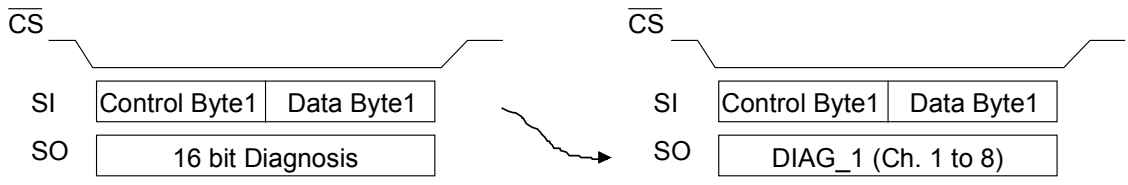
Serial Output (SO) data consists of 16 bit containing the diagnosis information for channels 1 to 8 with two bits per channel.
**DIAG_1:** Diagnosis data for channels 1 to 8.

Channel 9 to 16:

**Control Byte2:** Operation mode and diagnosis select for channels 9 to 16
**Data Byte2:** ON/OFF information for channel 9 to 16
**DIAG_2:** Diagnosis data for channels 9 to 16.

To drive all 16 channels and to get the complete diagnosis data of the TLE 6240 GP a two step access has to be performed as follows:

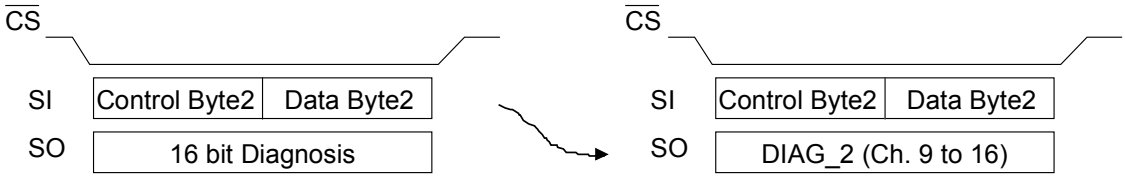
**First access:**




***SI command***: Control Byte 1 programs the operation mode of channels 1 to 8.
Data Byte 1 gives the input information (on or off) for Channel 1 to 8.
***SO diagnosis***: Diagnosis information of channel 1 to 8 or 9 to 16, depending on the SI control word before.

***SI command***: Control Byte 1 programs the operation mode of Channels 1 to 8.
Data Byte 1 gives the input information (on or off) for Channel 1 to 8.
***SO diagnosis***: 16 bit diagnosis information (two bit per channel) of channels 1 to 8

**Second access:**




***SI command***: Control Byte 2 programs the operation mode of channels 9 to 16.
Data Byte 2 gives the input information (on or off) for Channel 9 to 16.
***SO diagnosis***: Diagnosis information of channel 1 to 8 or 9 to 16, depending on the SI control word before.

***SI command***: Control Byte 2 programs the operation mode of Channels 9 to 16.
Data Byte 2 gives the input information (on or off) for Channel 9 to 16.
***SO diagnosis***: 16 bit diagnosis information (two bit per channel) of channels 9 to 16

## Detailed Description

As mentioned above, the serial input information consist of a control byte and a data byte. Via the control byte, the specific mode of the device is programmable.

MSB CCCCCCCC DDDDDDDD LSB : 16 bit serial input information
Control Byte Data Byte

Ten specific control words are recognised, having the following functions:

| No. | SI Contol and Data Byte | Function |
|---|---|---|
| 1 | LLLL LLLL XXXX XXXX | 'Full Diagnosis' (two bits per channel) performed for channels 1 to 8. No change to output states. |
| 2 | HHLL LLLL XXXX XXXX | State of the eight parallel inputs and '1-bit Diagnosis' for channel 1 to 8 is provided |
| 3 | HLHL LLLL XXXX XXXX | Echo-function of SPI; SI direct connected to SO |
| 4 | LLHH LLLL DDDDDDDD | IN1...4 and serial data bits 'OR'ed. 'Full Diagnosis' performed for channels 1 to 8. |
| 5 | HHHH LLLL DDDDDDDD | IN1...4 and serial data bits 'AND'ed. 'Full Diagnosis' performed for channels 1 to 8. |
| 6 | LLLL HHHH XXXX XXXX | 'Full Diagnosis' (two bits per channel) performed for channels 9 to 16. No change to output states. |
| 7 | HHLL HHHH XXXX XXXX | State of the eight parallel inputs and '1-bit Diagnosis' for channel 9 to 16 is provided. |
| 8 | HLHL HHHH XXXX XXXX | Echo-function of SPI; SI direct connected to SO |
| 9 | LLHH HHHH DDDDDDDD | IN9...12 and serial data bits 'OR'ed. 'Full Diagnosis' performed for channels 9 to 16. |
| 10 | HHHH HHHH DDDDDDDD | IN9...12 and serial data bits 'AND'ed. 'Full Diagnosis' performed for channels 9 to 16. |

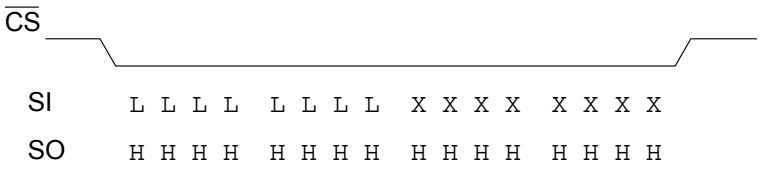
Note: Control Byte: Channel Selection via Bit 0 to 3
Bits 0 to 3 = L Channels 1 to 8 selected
Bits 0 to 3 = H Channels 9 to 16 selected
Data byte: 'X' means 'don't care', because this data bits will be ignored
'D' represents the data bits, either being H (= ON) or L (= OFF)

In the following section the different control bytes will be descriped. X used within the control byte means:

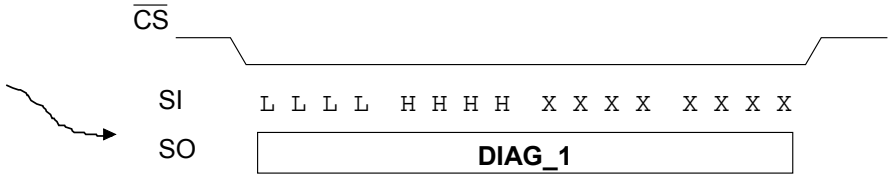
X = L: Command is valid for channels 1 to 8
X = H: Command is valid for channels 9 to 16

**1/6. LLLL XXXX** - Diagnosis only
By clocking in this control byte, it is possible to get pure diagnostic information (two bits per channel) in accordance with Figure 1 (page 14). The data bits are ignored, so that the state of the outputs are not influenced. This command is only active once unless the next control command is again "Diagnosis only". Diagnostic information can be read out at any time with no change of the switching conditions.

Example for two consecutive chip select cycles:




***SI command***: Diagnosis only for channels 1 to 8. No change of the output states
***SO diagnosis***: No fault, normal function of channels 1 to 8 or 9 to 16 depending on previous SI command




***SI command***: Diagnosis only for channels 9 to 16. No change of the output states **DIAG_2** provided during next chip select cycle
***SO diagnosis***: 2 bit diagnosis performed for channels 1 to 8

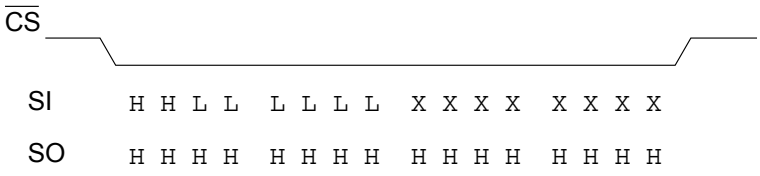
**2/7. HHLL XXXX** - Reading back of the eight inputs and '1-bit Diagnosis' provided
If the TLE 6240 GP is used as bare die in a hybrid application, it is necessary to know if proper connections exist between the µC-port and parallel inputs. By entering 'HHLL' as the control word, the first eight bits of the SO give the state of the parallel inputs, depending on the µC signals. By comparing the IN-bits with the corresponding µC-port signal, the necessary connection between the µC and the TLE 6240 GP can be verified - i.e. 'read back of the inputs'.
The second 8-bits fed out at the serial output contains '1-bit' fault information of the outputs (H = no fault, L = fault ). In the expression given below for the output byte, 'FX' is the fault bit for channel X.

MSB LSB

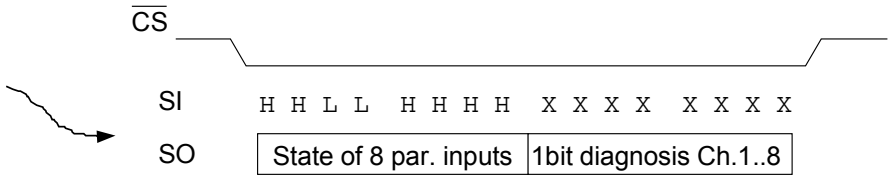
IN12 IN11 IN10 IN9 IN4 IN3 IN2 IN1 FX FX FX FX FX FX FX FX : Serial Output byte

Parallel Input Signals | Fault Bits Channels 1 to 8 or 9 to 16

Example for two consecutive chip select cycles:



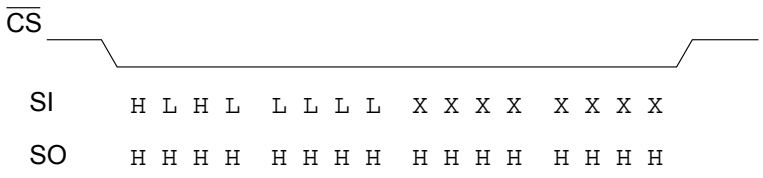

***SI command***: No change of the output states; reading back of the 8 inputs and 1bit diagnosis for channels 1 to 8
***SO diagnosis***: No fault, normal function of channels 1 to 8 or 9 to 16 depending on previous SI command



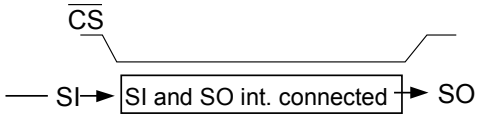

***SI command***: No change of the output states; reading back of the 8 inputs and 1bit diagnosis for channels 9 to 16 provided during next chip select cycle
***SO diagnosis***: State of eight parallel inputs and 1 bit diagnosis performed for channels 1 to 8

### 3/8. HLHL XXXX - Echo-function of SPI

To check the proper function of the serial interface the TLE 6240 GP provides a "SPI Echo Function". By entering HLHL as control word, SI and SO are connected during the next $\overline{CS}$ period. By comparing the bits clocked in with the serial output bits, the proper function of the SPI interface can be verified. This internal loop is **only closed once** (for one $\overline{CS}$ period). The “Echo Function” does not cause any internal processing of data and after the next $\overline{CS}$ signal the SO data is “0” (all registers reset).



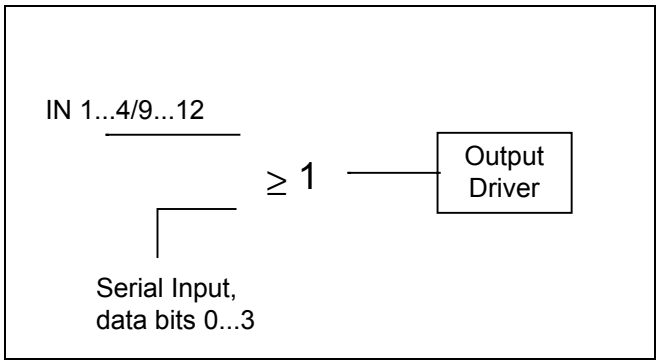

***SI command***: No change of the output states; Echo function of SPI
***SO diagnosis***: No fault, normal function of channels 1 to 8 or 9 to 16 depending on previous SI command




**Echo-function of SPI**, i.e. SI directly connected to SO.
SI information **will not be accepted during this cycle**.

### 4/9. LLHH XXXX DDDDDDDD - OR operation, and ‘full diagnosis’

With LLHH LLLL as the control word, each of the input signals IN1...IN4 are 'OR'ed with the corresponding SI data bits.
With LLHH HHHH as the control word, each of the input signals IN9...IN12 are 'OR'ed with the corresponding SI data bits.

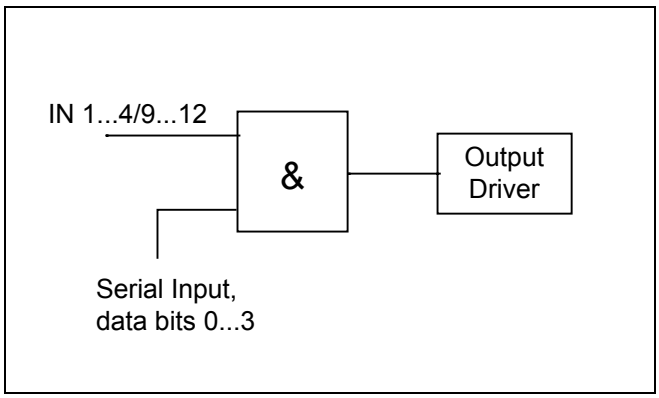



This OR operation enables the serial interface to switch the channel ON, even though the corresponding parallel input might be in the off state.

**SPI Priority for ON-State**

Also parallel control of the outputs is possible without an SPI input.
The OR-function is the default Boolean operation if the device restarts after a Reset, or when the supply voltage is switched on for the first time.
If the OR operation is programmed it is latched until it is overwritten by the AND operation.

**5/10. HHHH XXXX DDDDDDDD -** AND operation, and 'full diagnosis'
With HHHH LLLL as the control word, each of the input signals IN1...IN4 are 'AND'ed with the corresponding SI data bits.
With HHHH HHHH as the control word, each of the input signals IN9...IN12 are 'AND'ed with the corresponding SI data bits.




The AND operation implies that the output can be switched off by the SPI data bit input, even if the corresponding parallel input is in the ON state.

**SPI Priority for OFF-state**

This also implies that the serial input data bit can only switch the output channel ON if the corresponding parallel input is in the ON state.
If the AND operation is programmed it is latched until it is overwritten by the OR operation.

**Control words beside No. 1- 10**

Not specified Control words are not executed (cause no function) and the shift register (SO Data) is reset after the $\overline{\textbf{CS}}$ signal (all “0”).

*Example for an access to channel 1 to 8:*
LLHH LLLL HLLH LLLH: OR operation between parallel inputs and data bits, i.e channel 1, 5 and 8 will be switched on.
The next command is now: **LHHH LLLL HHHH LLLL**
LHHH LLLL as command word has no special meaning and will not be accepted. The output states will not be changed and the shift register will be reset (at the next $\overline{\textbf{CS}}$ SO Data all “0”).

## Diagnostics

$\overline{\textbf{FAULT}}$ - Fault pin. There is a general fault pin (open drain) which shows a high to low transition as soon as an error occurs for any one of the sixteen channels. This fault indication can be used to generate a µC interrupt. Therefore a ‘diagnosis’ interrupt routine need only be called after this fault indication. This saves processor time compared to a cyclic reading of the SO information.
As soon as a fault occurs, the fault information is latched into the diagnosis register. A new error will over-write the old error report. Serial data out pin (SO) is in a high impedance state when $\overline{CS}$ is high. If $\overline{CS}$ receives a LOW signal, all diagnosis bits can be shifted out serially.

For full diagnosis there are two diagnostic bits per channel configured as shown in Figure 1.

**Normal function:** The bit combination **HH** indicates that there is no fault condition, i.e. normal

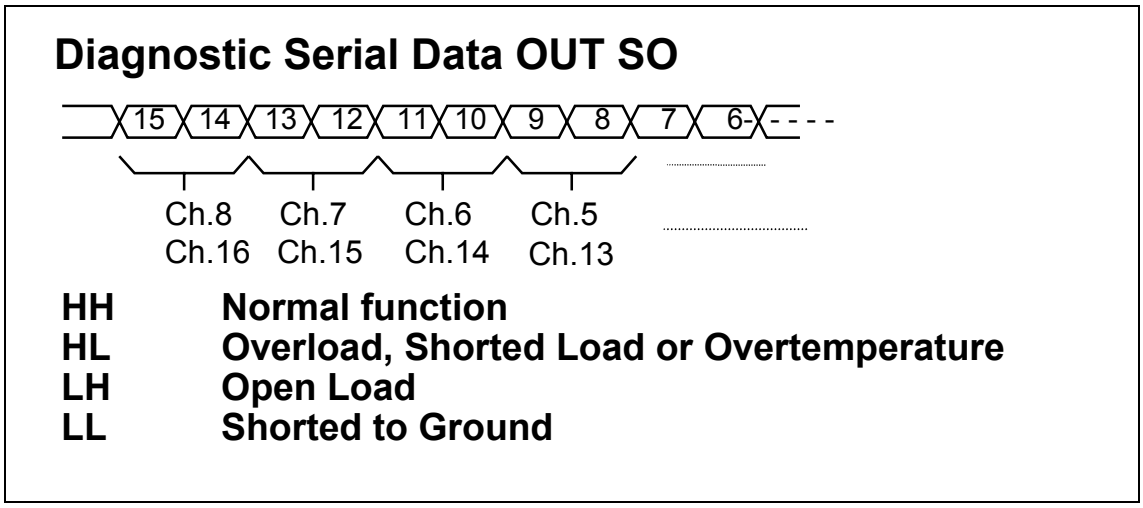



**Figure 1: Two bits per channel diagnostic feedback**

function.

**Overload, Short Circuit to Battery (SCB) or Overtemperature: HL** is set when the current limitation gets active, i.e. there is a overload, short to supply or overtemperature condition. **Open load:** An open load condition is detected when the drain voltage decreases below 3 V (typ.). **LH** bit combination is set.

**Short Circuit to GND:** If a drain to ground short circuit exists and the drain to ground current exceeds 100 µA, short to ground is detected and the **LL** bit combination is set.

A definite distinction between open load and short to ground is guaranteed by design.

The standard way of obtaining diagnostic information is as follows:
Clock in serial information into SI pin and wait approximately 150 µs to allow the outputs to settle. Clock in the identical serial information once again - during this process the data coming out at SO contains the bit combinations representing the diagnosis conditions as described in figure 1.

**Reset of the Diagnosis Register**

The diagnosis register is reset after reading the diagnosis data (after the falling $\overline{CS}$ edge). This is done for channels 1-8 and channels 9-16 separately depending on the previous command.

By means of the control byte it is possible either to:

a) control the outputs according to the data byte, as well as being able to read the diagnostic information (two bits per channel)
or b) purely get diagnostic information without changing the state of the outputs
or c) read back the parallel inputs plus a simple diagnosis (one bit per channel)
or d) SPI "Echo Function" as a diagnosis of proper SPI function

a) Serial Control of Outputs

- **LLHHLLLL LHLHHLLL**
  Control Byte Data Byte
  SI information: OR-operation valid for channels 1 to 8.
  SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle.

- **LLHHHHHH LHLHHLLL**
  Control Byte Data Byte
  SI information: OR-operation valid for channels 9 to 16
  SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle.

- **HHHHLLLL LHLHHLLL**
  Control Byte Data Byte
  SI information: AND-operation valid for channels 1 to 8
  SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle.

- **HHHHHHHH LHLHHLLL**
  Control Byte Data Byte
  SI information: AND-operation valid for channels 9 to 16
  SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle.

b) Diagnosis Only

- **LLLLLLLL XXXXXXXX**
  Control Byte Data Byte
  SI information: Full diagnosis for channels 1 to 8. No change of output states.
  SO: 16 bit diagnosis for channels 1 to 8 performed during next chip select cycle.

- **LLLLHHHH XXXXXXXX**
  Control Byte Data Byte
  SI information: Full diagnosis for channels 9 to 16. No change of output states.
  SO: 16 bit diagnosis for channels 9 to 16 performed during next chip select cycle.

c) Read back of parallel inputs plus simple diagnosis

- **HHLLLLLL XXXXXXXX** :
  Control Byte Data Byte
  SI information: No change of the output states. Read back of parallel inputs and 1 bit diag nosis for channels 1 to 8.
  SO:State of eight inputs plus 1 bit diagnosis for channel 1 to 8 during next chip select cycle.

- **HHLLHHHH XXXXXXXX**
  Control Byte Data Byte
  SI information: No change of the output states. Read back of parallel inputs and 1 bit diagnosis for channels 9 to 16.
  SO: State of eight inputs plus 1 bit diagnosis for channel 9 to 16 during next chip select cycle.

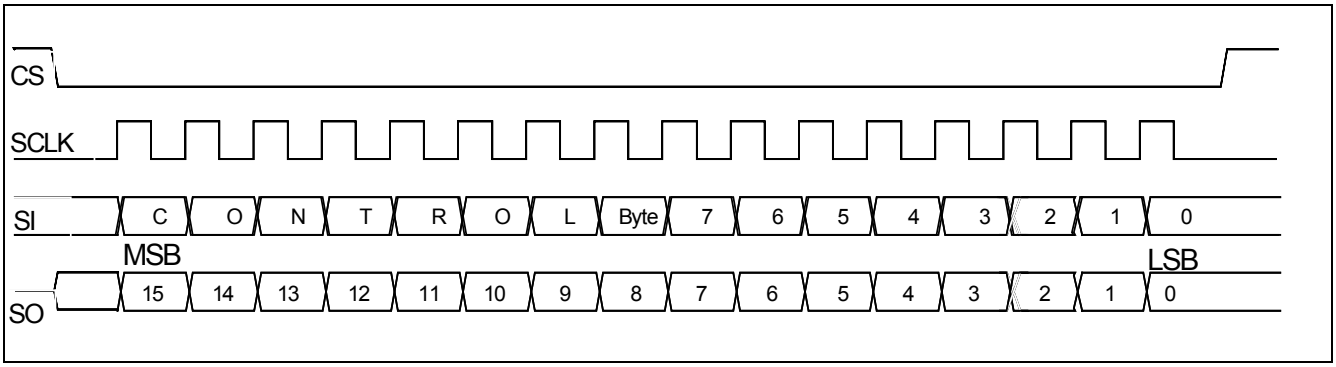
d) SPI Echo function

- **HLHLLLLL XXXXXXXX** :
  Control Byte Data Byte
  SI information: Echo function of SPI interface. No change of the output states.
  SO: During next chip select cycle the SI bits clocked in appear directly at SO because of an internal connection for this cycle

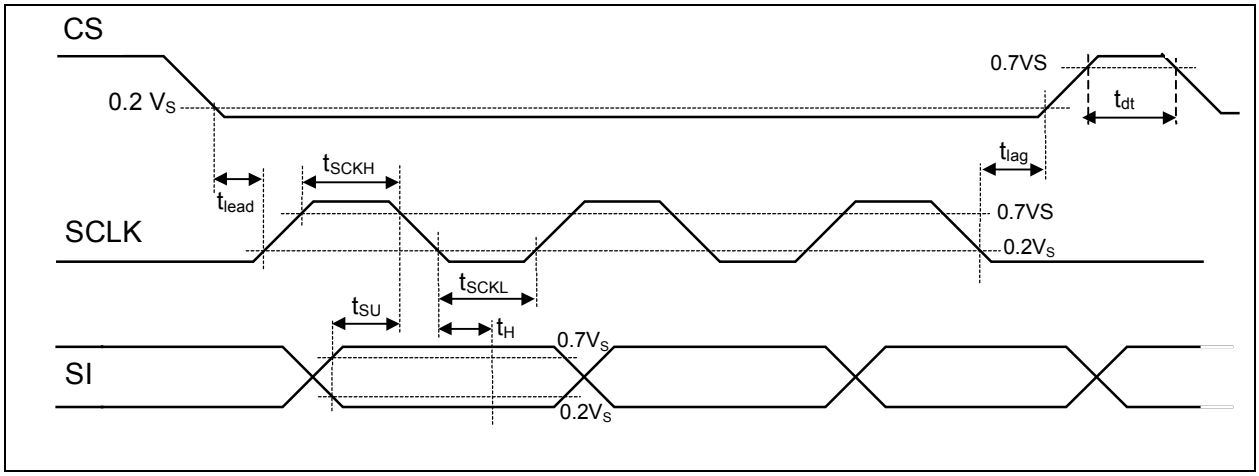
- **HLHLHHHH XXXXXXXX**
  Control Byte Data Byte
  SI information: Echo function of SPI interface. No change of the output states.
  SO: During next chip select cycle the SI bits clocked in appear directly at SO because of an internal connection for this cycle

# Timing Diagrams

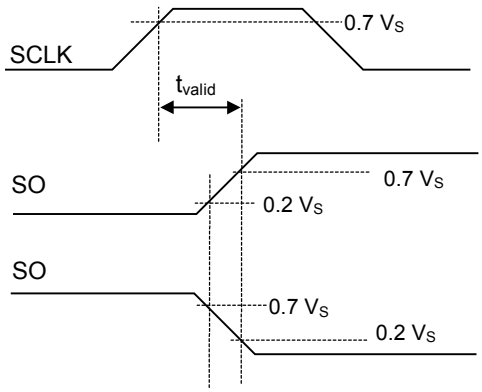
## Serial Interface



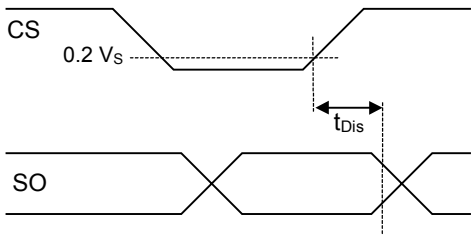

## Input Timing Diagram



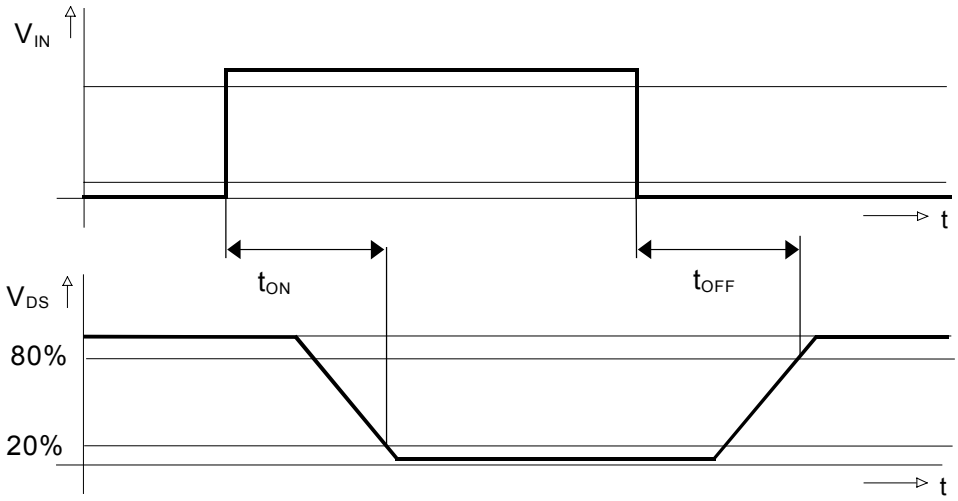

## SO Valid Time Waveforms



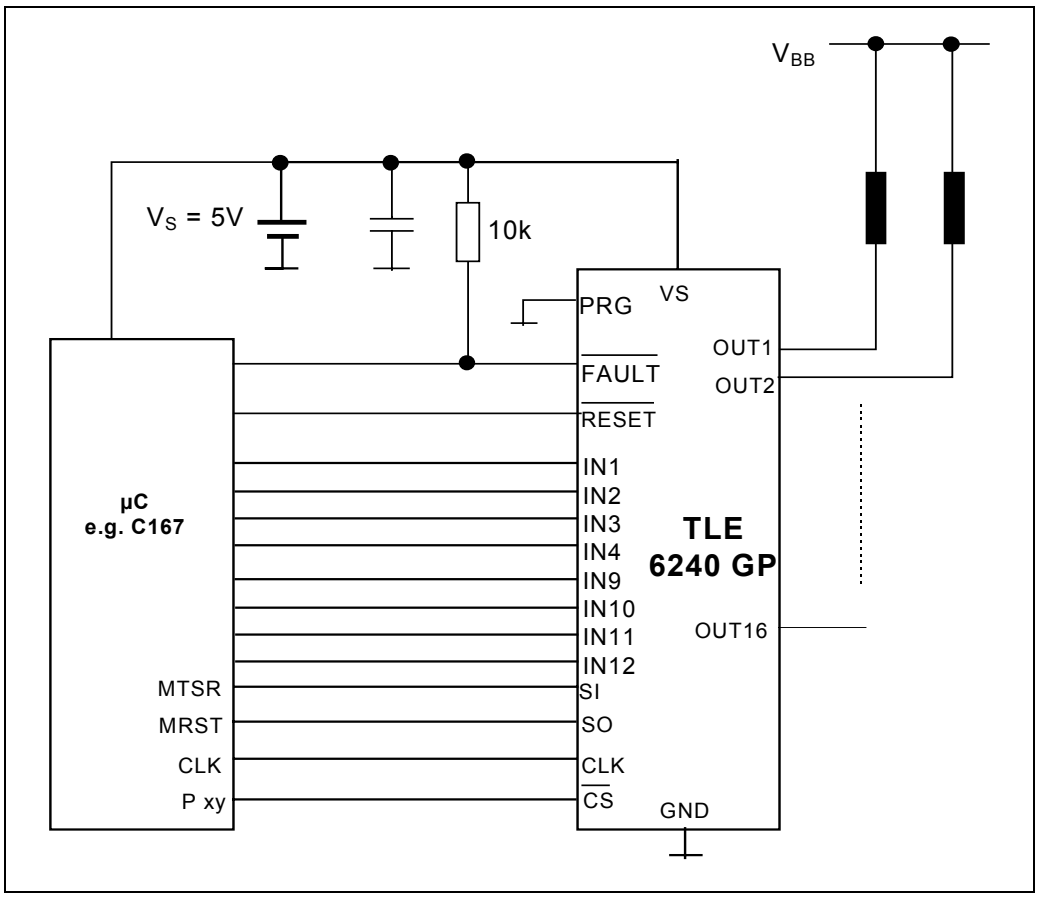

## Enable and Disable Time Waveforms



### Power Outputs




## Application Circuit



# Typical electrical Characteristics

## Drain-Source on-resistance

$R_{DS(ON)} = f(T_j)$ ; $V_s = 5V$

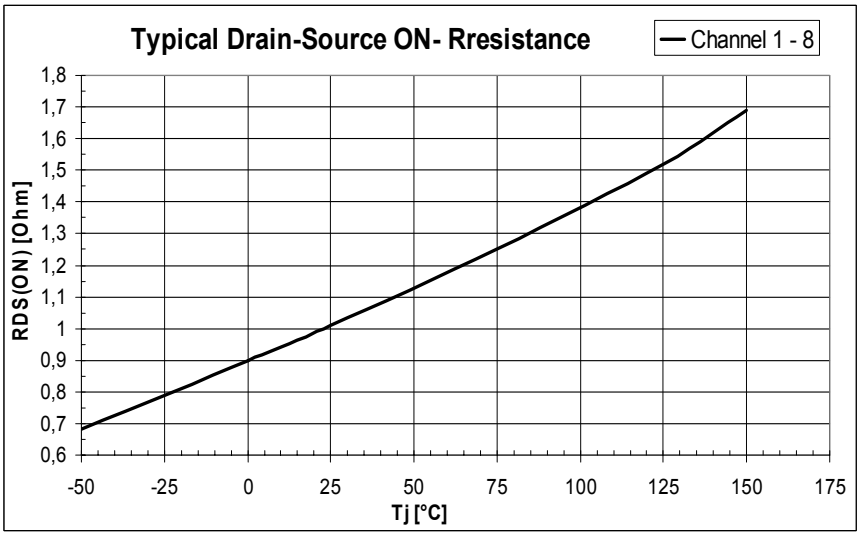



**Figure 2 :**
Typical ON Resistance versus Junction-Temperature

Channel 1-8

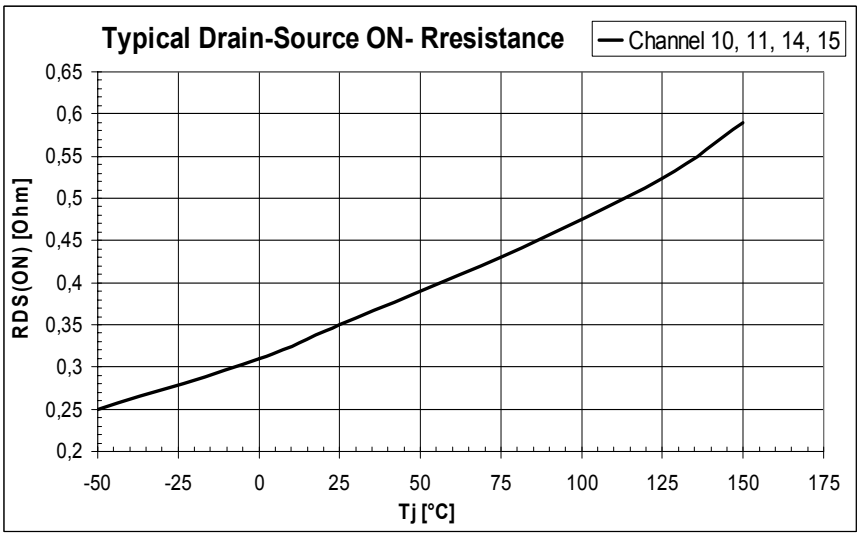



**Figure 3 :**
Typical ON Resistance versus Junction-Temperature

Channel 10, 11, 14, 15

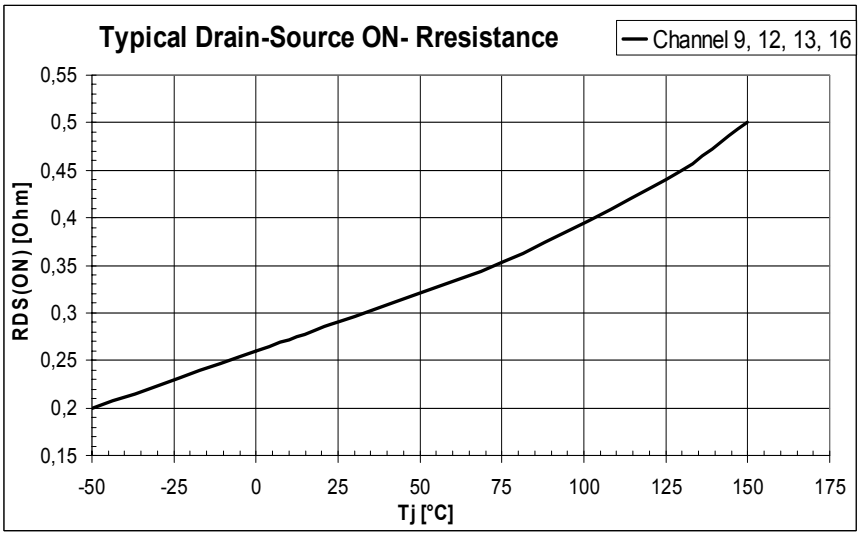



**Figure 4 :**
Typical ON Resistance versus Junction-Temperature

Channel 9, 12, 13, 16

## Output Clamping Voltage

$V_{DS(AZ)} = f(T_j)$ ; $V_s = 5V$

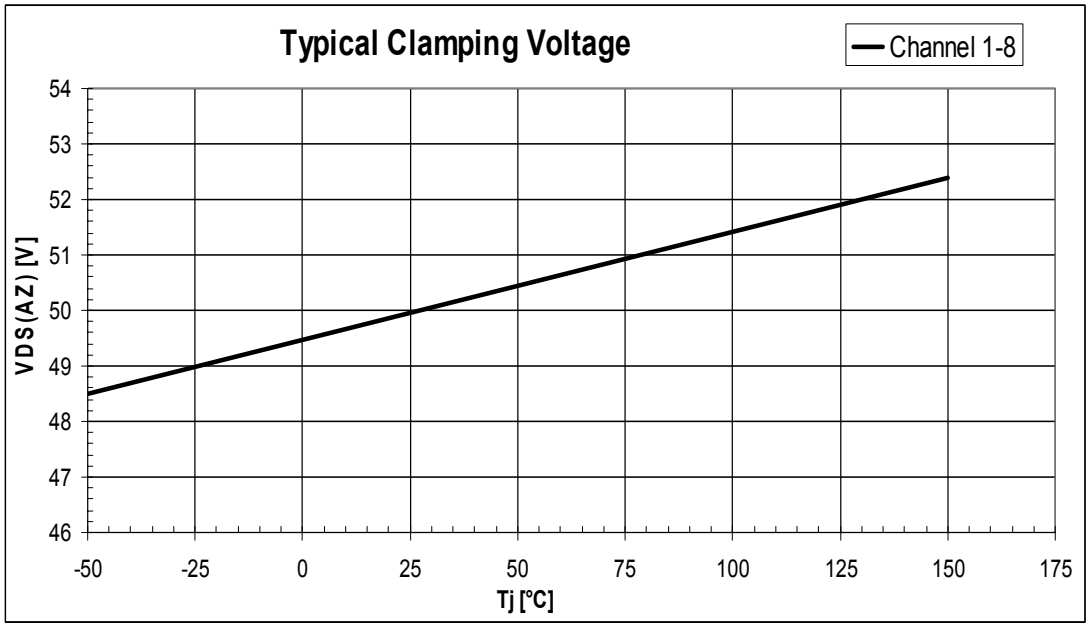



**Figure 5 :** Typical Clamping Voltage versus Junction-Temperature Channel 1-8

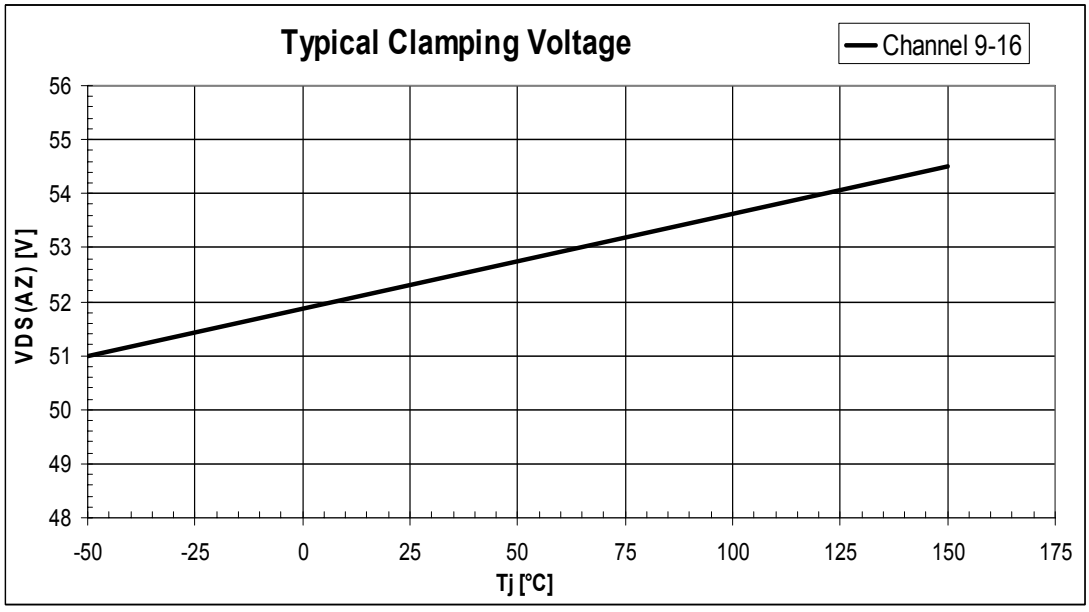
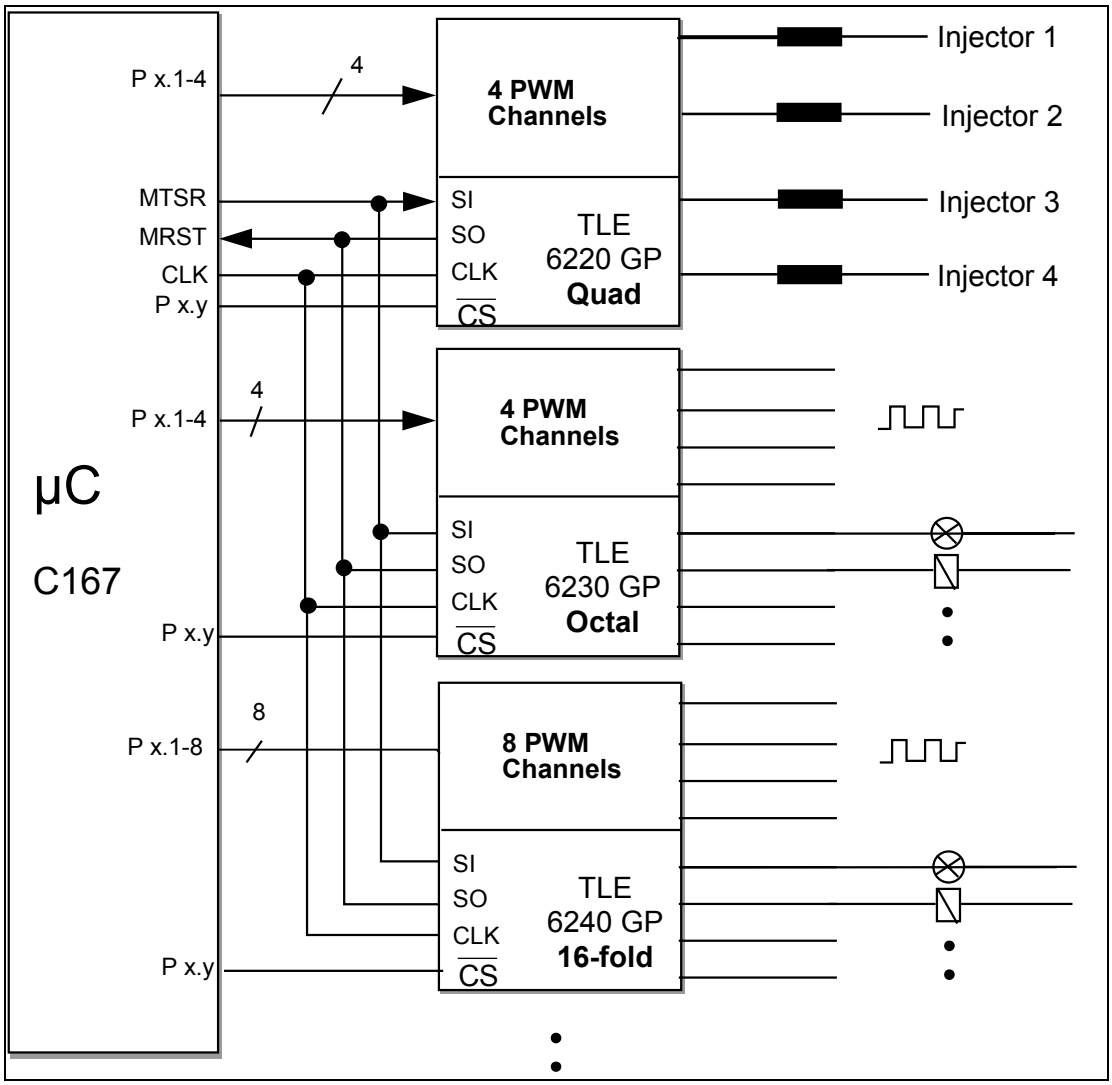



**Figure 6 :** Typical Clamping Voltage versus Junction-Temperature Channel 9-16

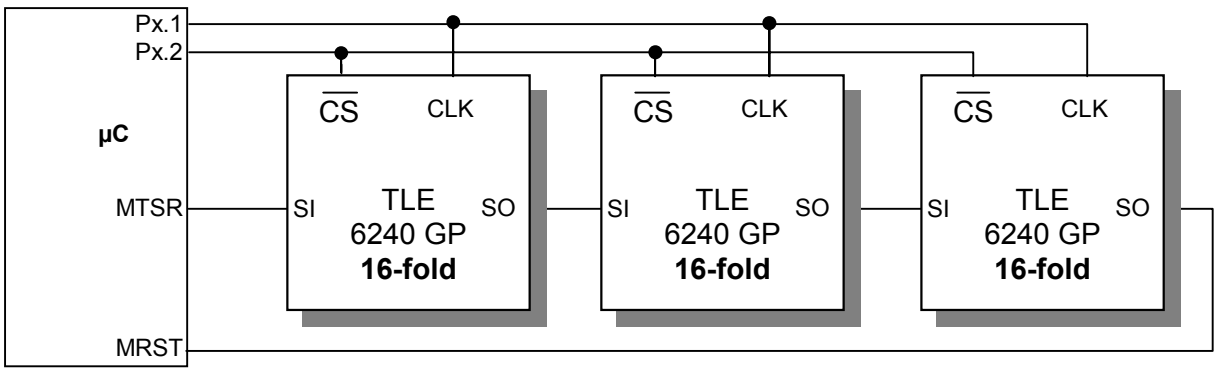
# Parallel SPI Configuration

## Engine Management Application

TLE 6240 GP in combination with TLE 6230 GP (octal switch) for relays and general purpose loads and TLE 6220 GP to drive the injector valves. This arrangement covers the numerous loads to be driven in a modern Engine Management/Powertrain system. From 28 channels in sum 16 can be controlled direct in parallel for PWM applications.



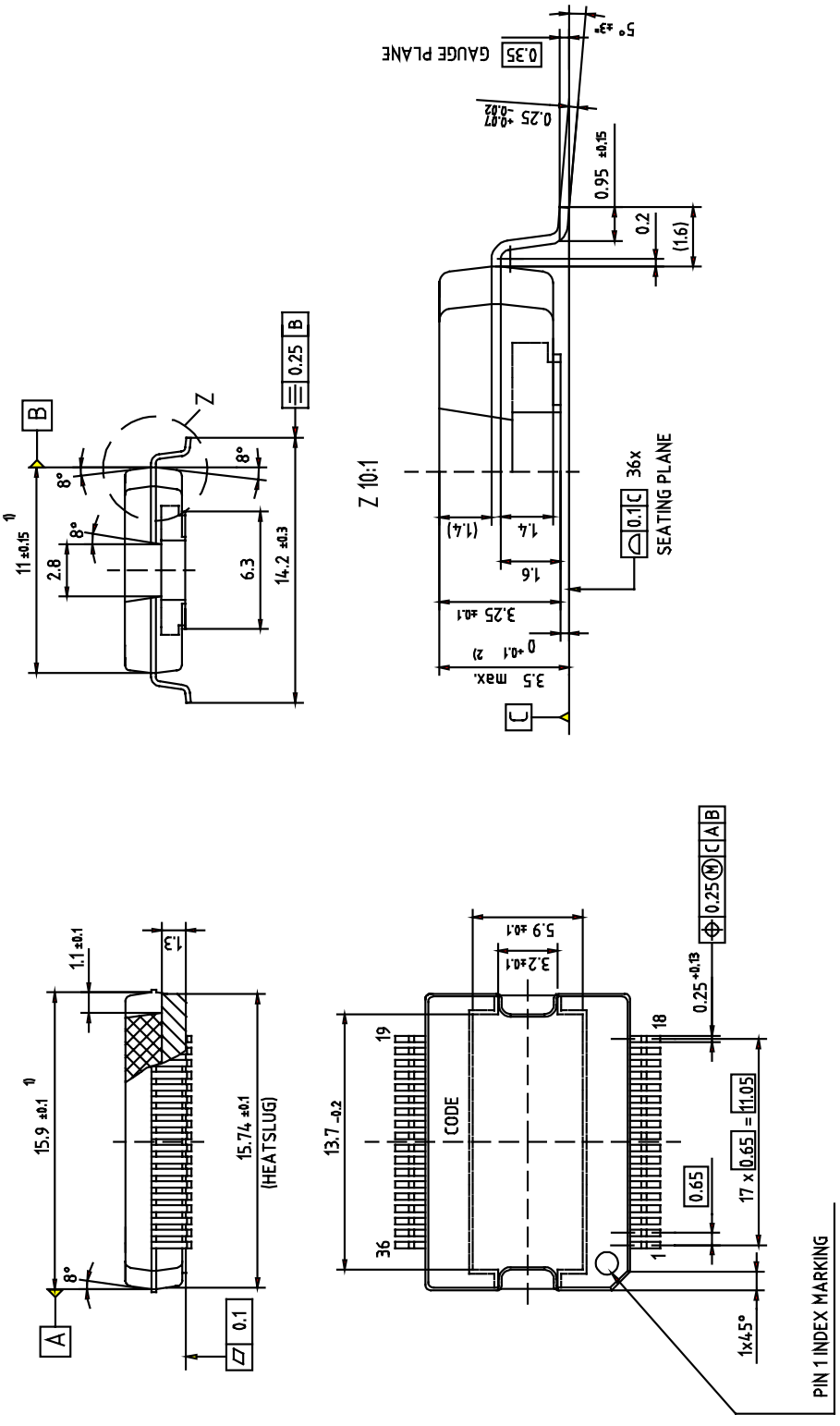

## Daisy Chain Application TLE 6240 GP



# Package and Ordering Code

**(all dimensions in mm)**

| P-DSO 36-12 | Ordering Code |
|---|---|
| TLE 6240 GP | Q67007-A9470 |



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