MCP616/7/8/9

2.3V to 5.5V Micropower Bi-CMOS Op Amps

Features

- Low Input Offset Voltage: ±150 µV (max.)
- Low Noise: 2.2 μV_{P-P} (typ., 0.1 Hz to 10 Hz)
- Rail-to-Rail Output
- Low Input Offset Current: 0.3 nA (typ.)
- Low Quiescent Current: 25 µA (max.)
- Power Supply Voltage: 2.3V to 5.5V
- Unity Gain Stable
- Chip Select ($\overline{CS}$) Capability: MCP618
- Industrial Temperature Range: -40°C to +85°C
- No Phase Reversal
- Available in Single, Dual and Quad Packages

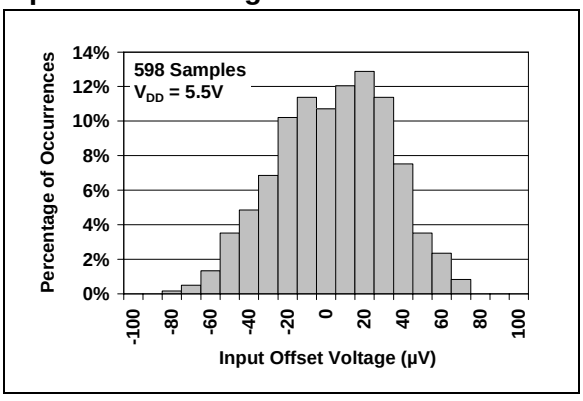
Typical Applications

- Battery Power Instruments
- Weight Scales
- Strain Gauges
- Medical Instruments
- Test Equipment

Available Tools

- SPICE Macro Models (at www.microchip.com)
- FilterLab® Software (at www.microchip.com)

Input Offset Voltage

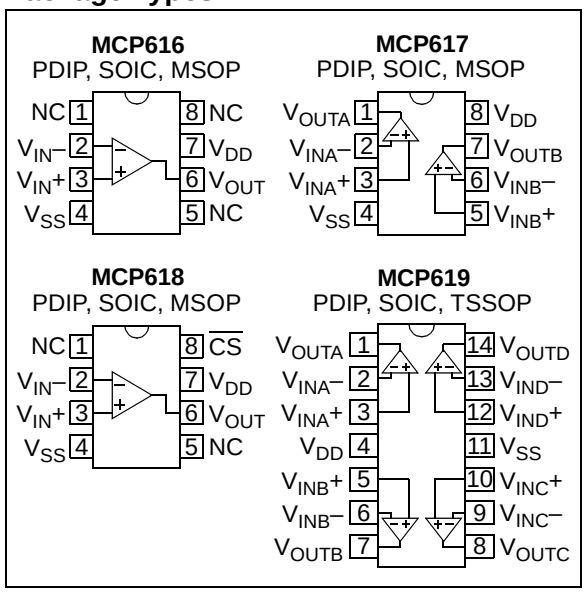


Description

The MCP616/7/8/9 family of operational amplifiers (op amps) from Microchip Technology Inc. are capable of precision, low-power, single-supply operation. These op amps are unity-gain stable, have low input offset voltage (±150 µV, max.), rail-to-rail output swing and low input offset current (0.3 nA, typ.). These features make this family of op amps well suited for battery-powered applications.

The single MCP616, the single MCP618 with Chip Select ($\overline{CS}$) and the dual MCP617 are all available in standard 8-lead PDIP, SOIC and MSOP packages. The quad MCP619 is offered in standard 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C, with power supplies from 2.3V to 5.5V.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 7.0V
All Inputs and Outputs ..... $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Input Pins .....±2 mA
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....-65°C to +150°C
Maximum Junction Temperature (T_J) .....+150°C
ESD protection on all pins (HBM;MM) .....4 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$ and R_L = 100 kΩ to $V_{DD}/2$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	–150	—	+150	µV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +85°C
Power Supply Rejection	PSRR	86	105	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	-35	-15	-5	nA	
At Temperature	I_B	-70	-21	—	nA	T_A = -40°C
At Temperature	I_B	—	-12	—	nA	T_A = +85°C
Input Offset Current	I_{OS}	—	±0.15	—	nA	
Common Mode Input Impedance	Z_{CM}	—	600||4	—	MΩ||pF	
Differential Input Impedance	Z_{DIFF}	—	3||2	—	MΩ||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS}		$V_{DD} - 0.9$	V	
Common Mode Rejection Ratio	CMRR	80	100	—	dB	V_{DD} = 5.0V, V_{CM} = 0.0V to 4.1V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	100	120	—	dB	R_L = 25 kΩ to $V_{DD}/2$, V_{OUT} = 0.05V to V_{DD} – 0.05V
DC Open-Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 5 kΩ to $V_{DD}/2$, V_{OUT} = 0.1V to V_{DD} – 0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 20	mV	R_L = 25 kΩ to $V_{DD}/2$, 0.5V output overdrive
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} – 60	mV	R_L = 5 kΩ to $V_{DD}/2$, 0.5V output overdrive
Linear Output Voltage Range	V_{OUT}	V_{SS} + 50	—	V_{DD} – 50	mV	R_L = 25 kΩ to $V_{DD}/2$, $A_{OL} \geq$ 100 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} – 100	mV	R_L = 5 kΩ to $V_{DD}/2$, $A_{OL} \geq$ 95 dB
Output Short Circuit Current	I_{SC}	—	±7	—	mA	V_{DD} = 2.3V
	I_{SC}	—	±17	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.3	—	5.5	V	
Quiescent Current per Amplifier	I_Q	12	19	25	µA	I_O = 0

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	190	—	kHz	
Phase Margin	PM	—	57	—	°	G = +1
Slew Rate	SR	—	0.08	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	2.2	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	32	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	70	—	fA/√Hz	f = 1 kHz

MCP618 $\overline{\text{CHIP SELECT}}$ ($\overline{\text{CS}}$) ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{CS}}$ Low Specifications						
$\overline{\text{CS}}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{\text{CS}}$ Input Current, Low	I_{CSL}	–1.0	0.01	—	µA	$\overline{\text{CS}}$ = V_{SS}
$\overline{\text{CS}}$ High Specifications						
$\overline{\text{CS}}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{\text{CS}}$ Input Current, High	I_{CSH}	—	0.01	2	µA	$\overline{\text{CS}}$ = V_{DD}
GND Current	I_{SS}	-2	-0.05	—	µA	$\overline{\text{CS}}$ = V_{DD}
Amplifier Output Leakage	$I_{O(LEAK)}$	—	10	—	nA	$\overline{\text{CS}}$ = V_{DD}
$\overline{\text{CS}}$ Dynamic Specifications						
$\overline{\text{CS}}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	9	100	µs	$\overline{\text{CS}}$ = 0.2V_{DD} to V_{OUT} = 0.9(V_{DD}/2), G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{\text{CS}}$ High to Amplifier Output High-Z	t_{OFF}	—	0.1	—	µs	$\overline{\text{CS}}$ = 0.8V_{DD} to V_{OUT} = 0.1(V_{DD}/2), G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{\text{CS}}$ Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V

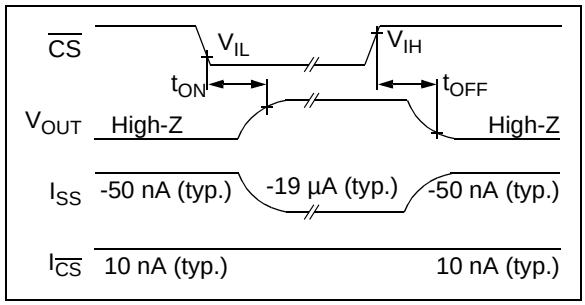


FIGURE 1-1: *Timing Diagram for the $\overline{\text{CS}}$ Pin on the MCP618.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP616/7/8/9 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

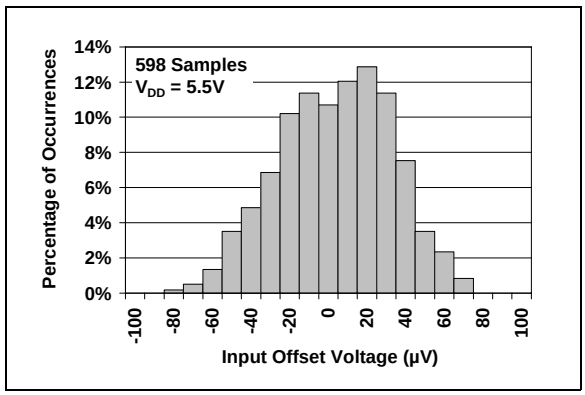


FIGURE 2-1: *Input Offset Voltage at V_{DD} = 5.5V.*

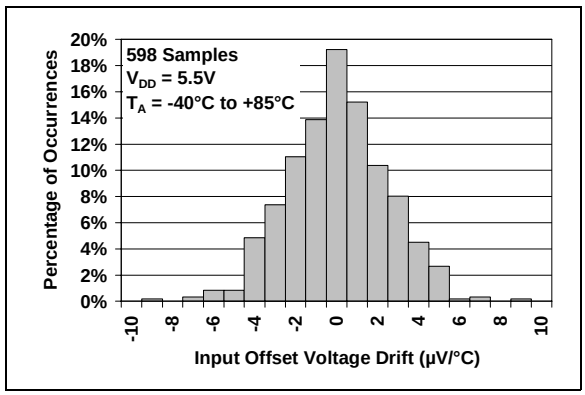


FIGURE 2-4: *Input Offset Voltage Drift at V_{DD} = 5.5V.*

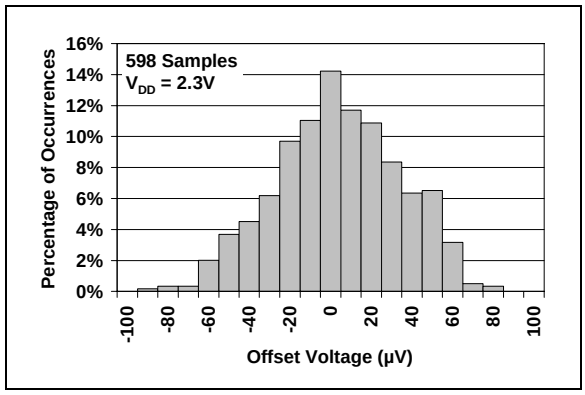


FIGURE 2-2: *Input Offset Voltage at V_{DD} = 2.3V.*

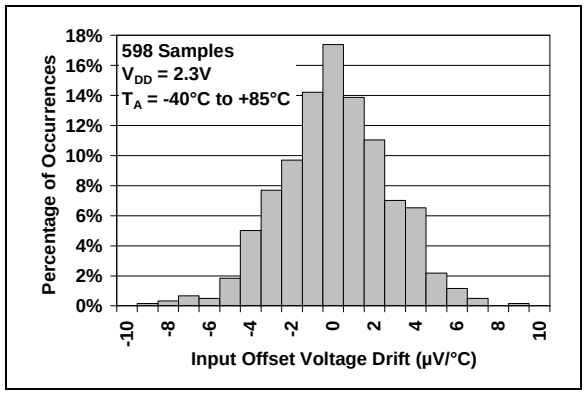


FIGURE 2-5: *Input Offset Voltage Drift at V_{DD} = 2.3V.*

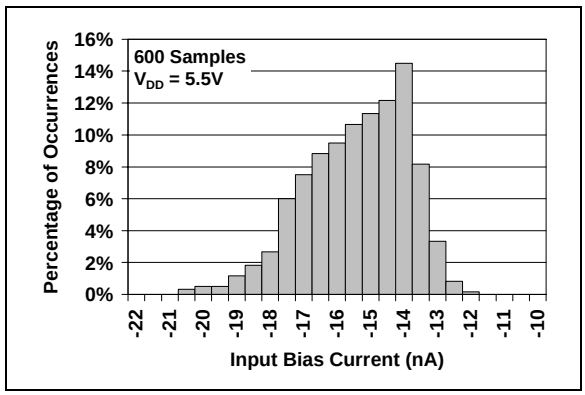


FIGURE 2-3: *Input Bias Current at V_{DD} = 5.5V.*

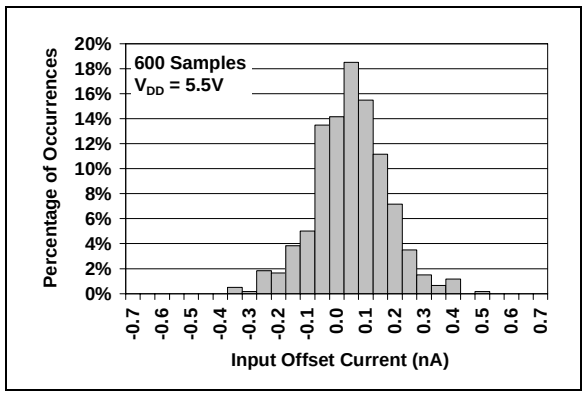


FIGURE 2-6: *Input Offset Current at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

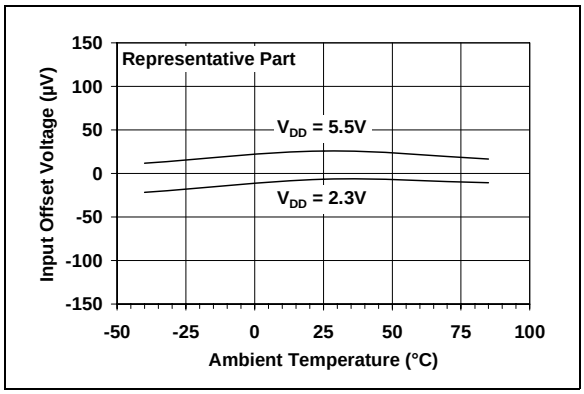


FIGURE 2-7: *Input Offset Voltage vs. Ambient Temperature.*

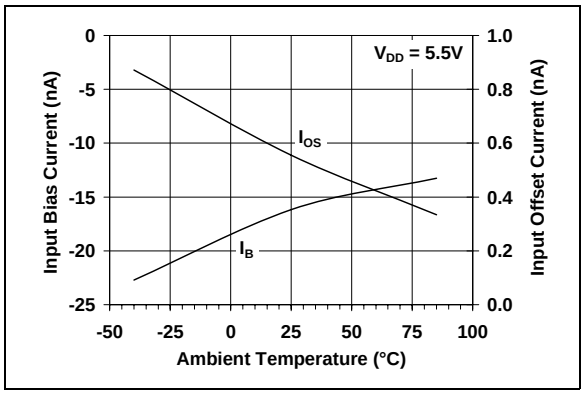


FIGURE 2-10: *Input Bias, Offset Currents vs. Ambient Temperature.*

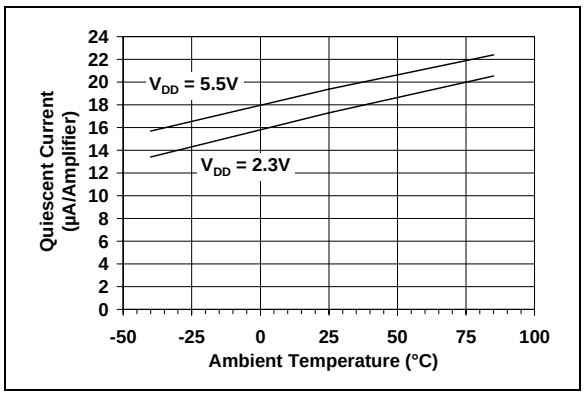


FIGURE 2-8: *Quiescent Current vs. Ambient Temperature.*

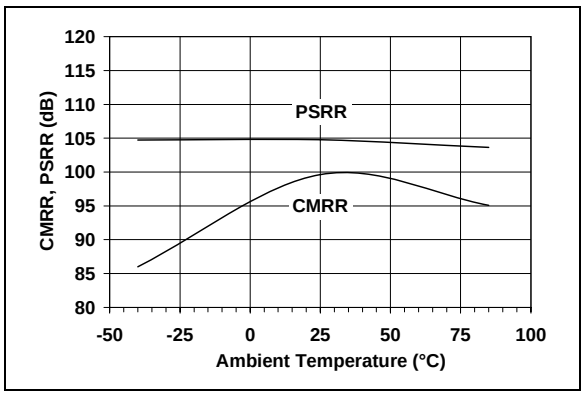


FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

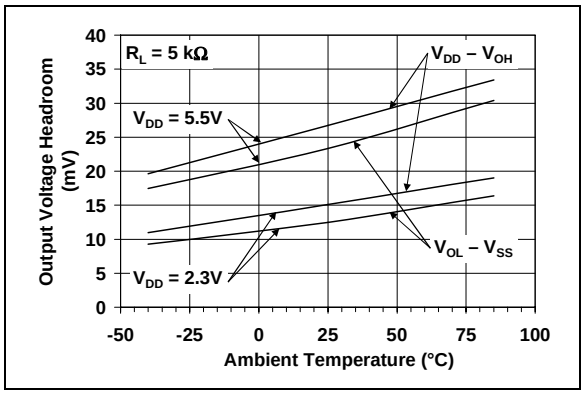


FIGURE 2-9: *Maximum Output Voltage Swing vs. Ambient Temperature at R_L = 5 kΩ.*

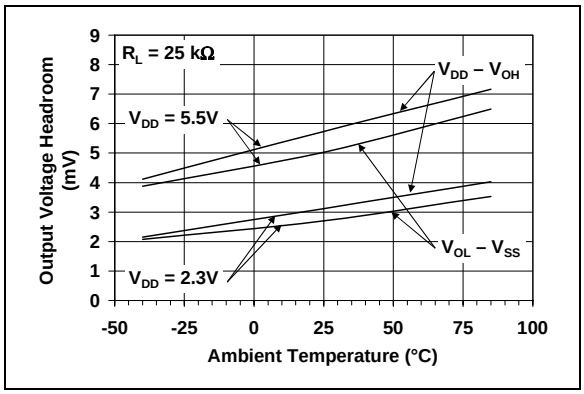


FIGURE 2-12: *Maximum Output Voltage Swing vs. Ambient Temperature at R_L = 25 kΩ.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

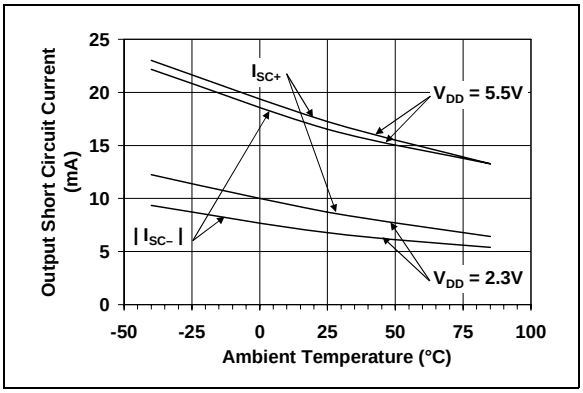


FIGURE 2-13: *Output Short Circuit Current vs. Ambient Temperature.*

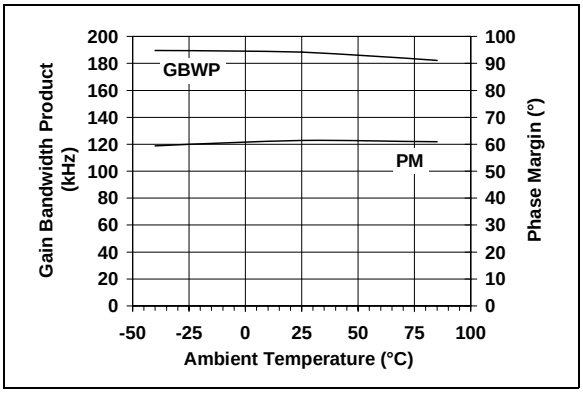


FIGURE 2-16: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

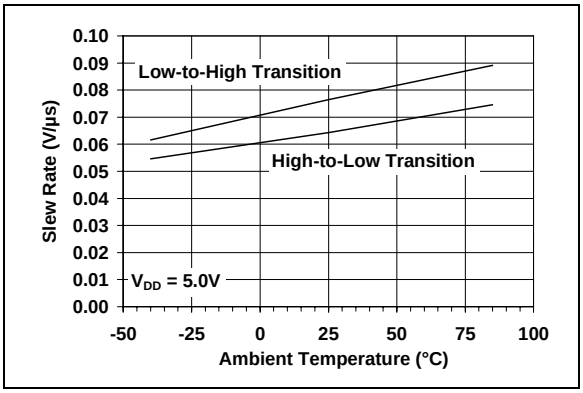


FIGURE 2-14: *Slew Rate vs. Ambient Temperature.*

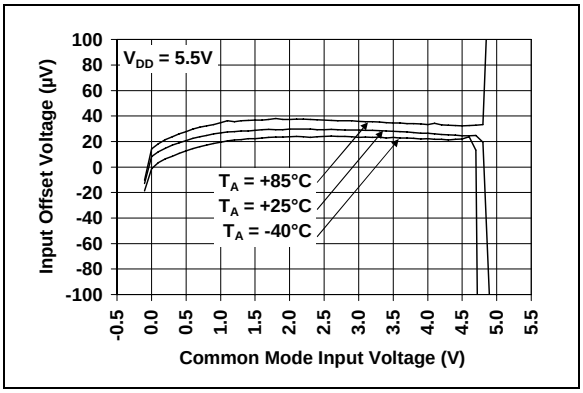


FIGURE 2-17: *Input Offset Voltage vs. Common Mode Input Voltage.*

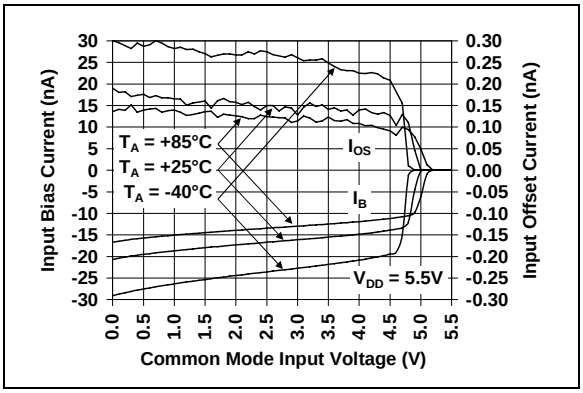


FIGURE 2-15: *Input Bias, Offset Currents vs. Common Mode Input Voltage.*

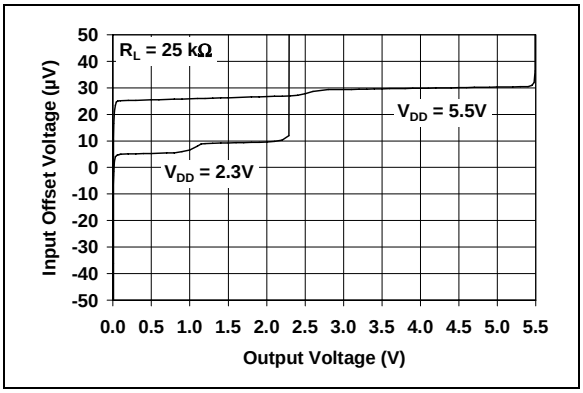


FIGURE 2-18: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

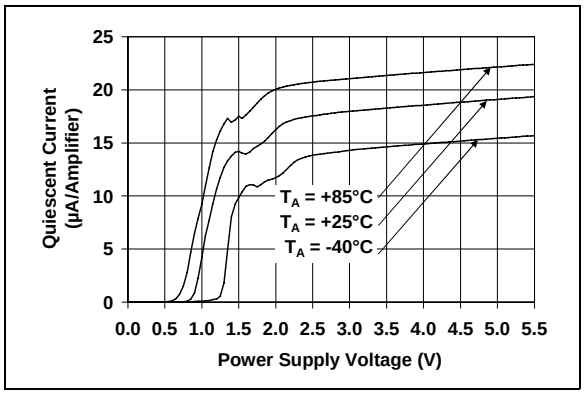


FIGURE 2-19: *Quiescent Current vs. Power Supply Voltage.*

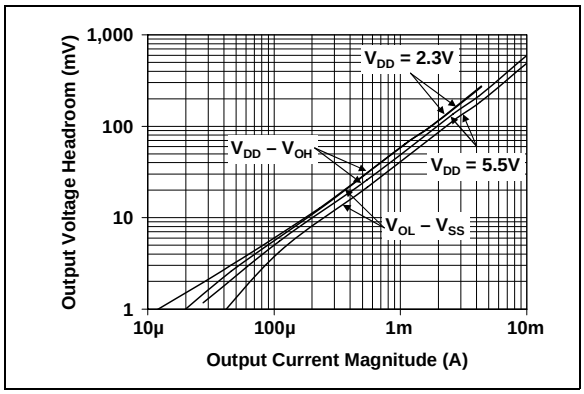


FIGURE 2-22: *Output Voltage Headroom vs. Output Current Magnitude*.

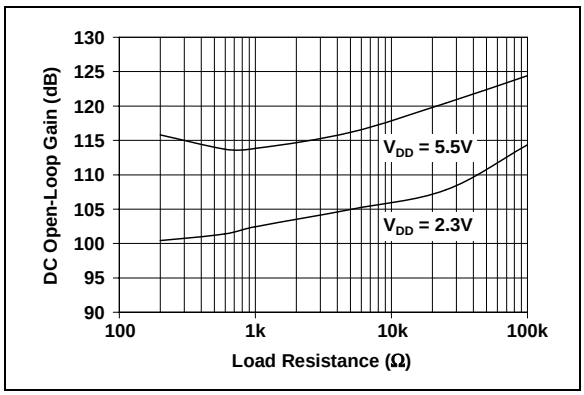


FIGURE 2-20: *DC Open-Loop Gain vs. Load Resistance.*

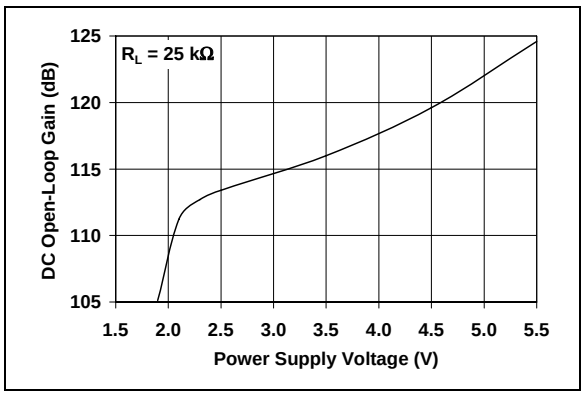


FIGURE 2-23: *DC Open-Loop Gain vs. Power Supply Voltage.*

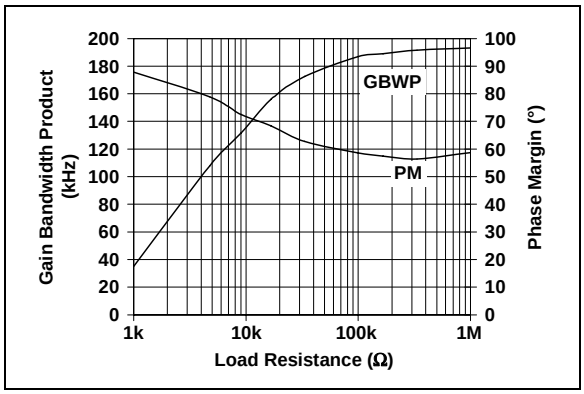


FIGURE 2-21: *Gain-Bandwidth Product, Phase Margin vs. Load Resistance.*

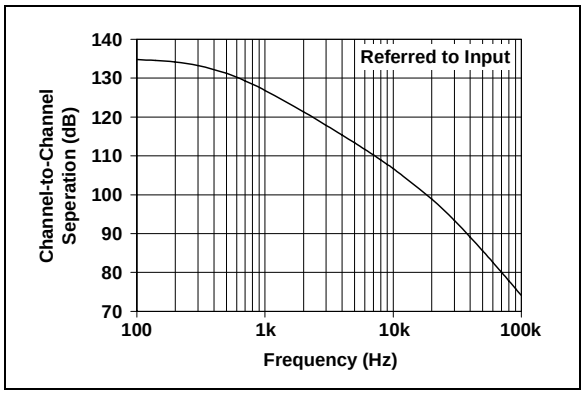


FIGURE 2-24: *Channel-to-Channel Separation vs. Frequency (MCP617 and MCP619 only).*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

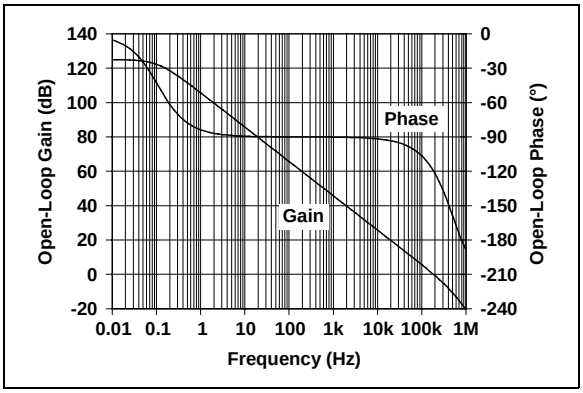


FIGURE 2-25: *Open-Loop Gain, Phase vs. Frequency.*

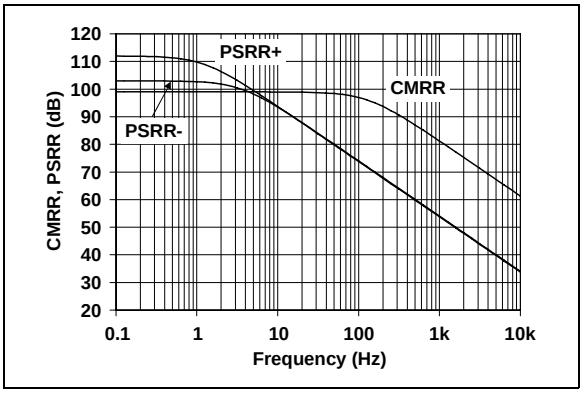


FIGURE 2-28: *CMRR, PSRR vs. Frequency.*

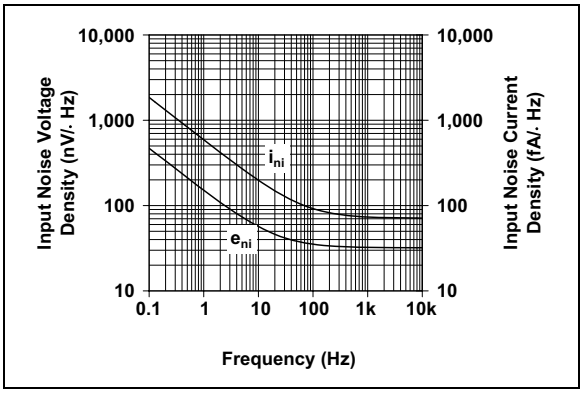


FIGURE 2-26: *Input Noise Voltage, Current Densities vs. Frequency.*

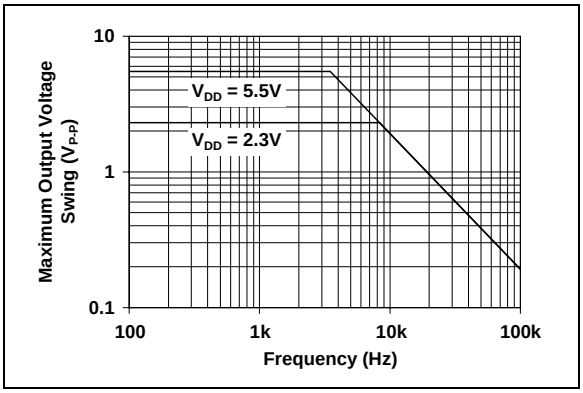


FIGURE 2-29: *Maximum Output Voltage Swing vs. Frequency.*

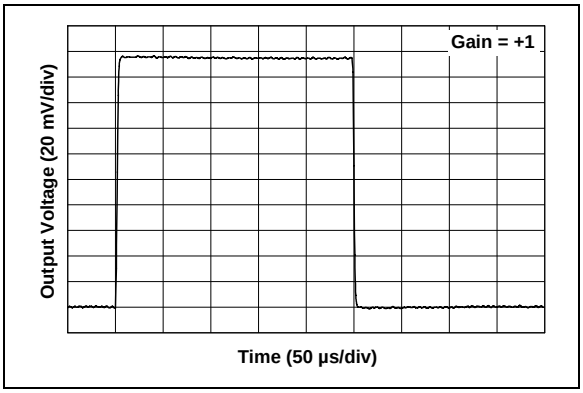


FIGURE 2-27: *Small-Signal, Non-Inverting Pulse Response.*

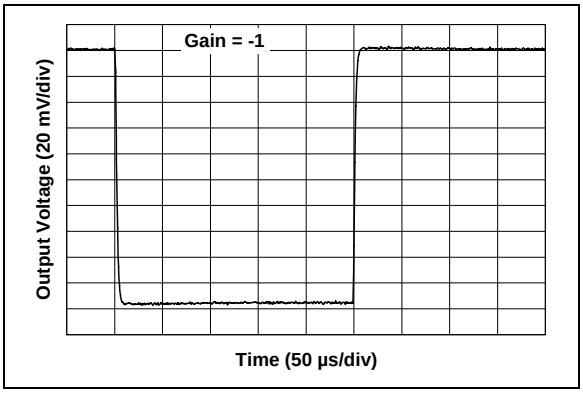


FIGURE 2-30: *Small-Signal, Inverting Pulse Response.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

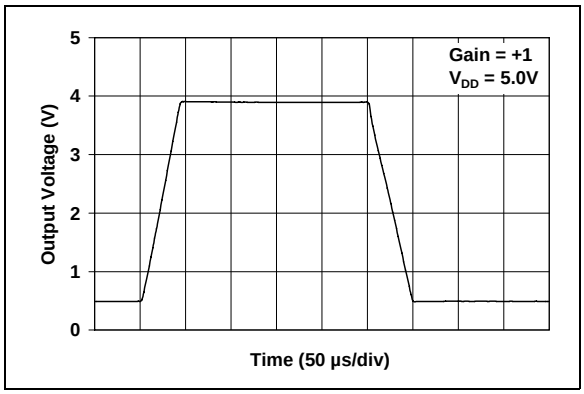


FIGURE 2-31: *Large-Signal, Non-Inverting Pulse Response.*

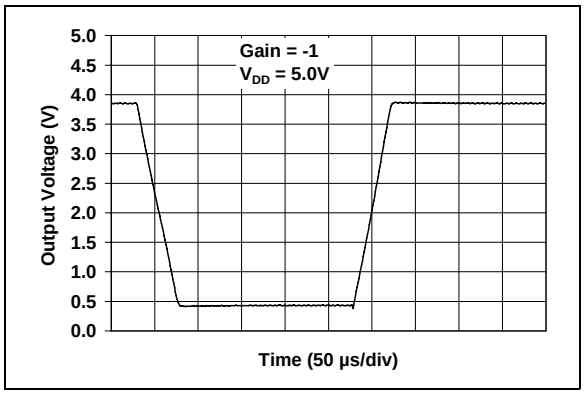


FIGURE 2-34: *Large-Signal, Inverting Pulse Response.*

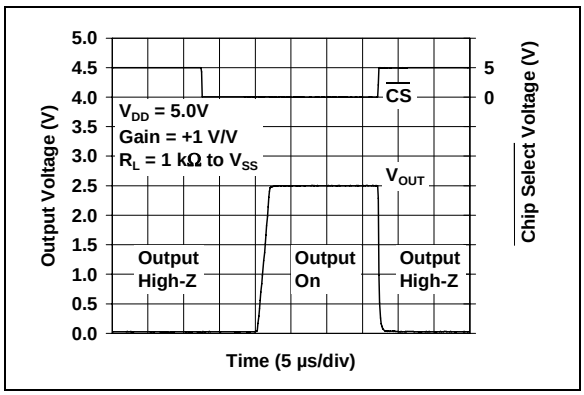


FIGURE 2-32: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP618 only).*

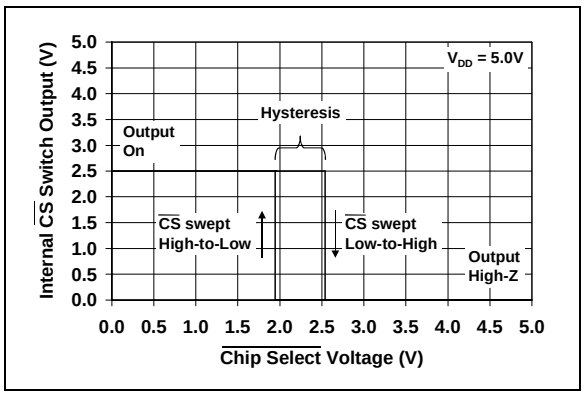


FIGURE 2-35: *Chip Select ($\overline{CS}$) Internal Hysteresis (MCP618 only).*

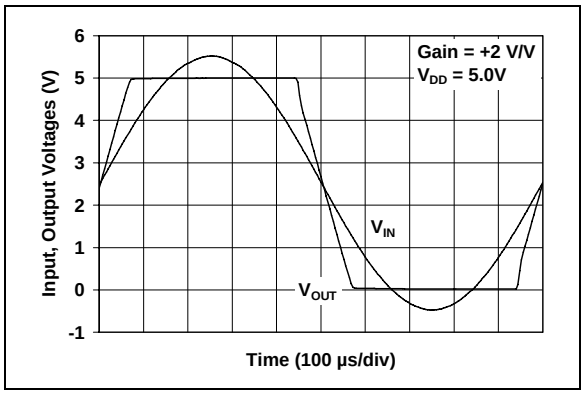


FIGURE 2-33: *The MCP616/7/8/9 Show No Phase Reversal.*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP616	MCP617	MCP618	MCP619	Symbol	Description
6	1	6	1	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
7	8	7	4	V_{DD}	Positive Power Supply
—	5	—	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	6	—	6	$V_{INB}-$	Inverting Input (op amp B)
—	7	—	7	V_{OUTB}	Output (op amp B)
—	—	—	8	V_{OUTC}	Output (op amp B)
—	—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	—	14	V_{OUTD}	Output (op amp D)
—	—	8	—	$\overline{CS}$	$\overline{\text{Chip Select}}$
1, 5, 8	—	1, 5	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance PNP inputs with low bias currents.

3.3 $\overline{\text{Chip Select}}$ Digital Input ($\overline{CS}$)

This is a CMOS, Schmitt-triggered input that places the MCP618 op amp into a low-power mode of operation.

3.4 Power Supply (V_{SS} and V_{DD})

The positive power supply (V_{DD}) is 2.5V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are between V_{SS} and V_{DD}.

Typically, these parts are used in a single-supply (positive) configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These parts should use a bulk capacitor (typically 1 µF or larger) within 100 mm of the V_{DD} pin; it can be shared with nearby analog parts.

4.0 APPLICATIONS INFORMATION

The MCP616/7/8/9 family of op amps is manufactured using Microchip's state-of-the-art CMOS process, which includes PNP transistors. These op amps are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Inputs

The MCP616/7/8/9 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-33 shows the input voltage exceeding the supply voltage without any phase reversal.

The inputs of the MCP616/7/8/9 op amps connect to a differential PNP input stage. The Common Mode Input Voltage Range (V_{CMR}) includes ground in single-supply systems (V_{SS}), but does not include V_{DD}. This means that the amplifier input behaves linearly as long as the Common Mode Input Voltage (V_{CM}) is kept within the specified limits (V_{SS} to V_{DD} – 0.9V at +25°C).

Input voltages that exceed the Absolute Maximum Voltage Range (V_{SS} – 0.3V to V_{DD} + 0.3V) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 4-1.

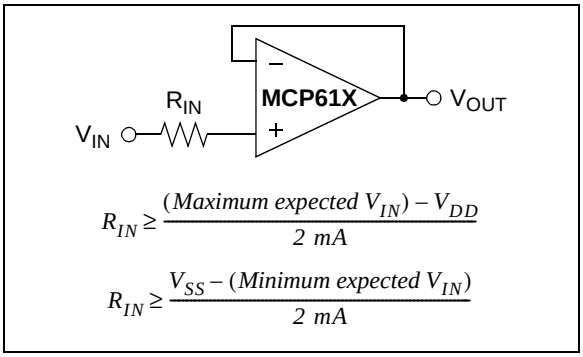


FIGURE 4-1: *Input Current-Limiting Resistor (R_{IN}).*

4.2 DC Offsets

The MCP616/7/8/9 family of op amps have a PNP input differential pair that gives good DC performance. They have very low input offset voltage (±150 µV, max.) at T_A = +25°C, with a typical bias current of -15 nA (sourced out of the inputs).

There must be a DC path to ground (or power supply) from both inputs, or the op amp will not bias properly. The DC resistances seen by the op amp inputs ($R_1||R_2$ and $R_4||R_5$ in Figure 4-2) need to be equal and less than 100 kΩ, to minimize the total DC offset.

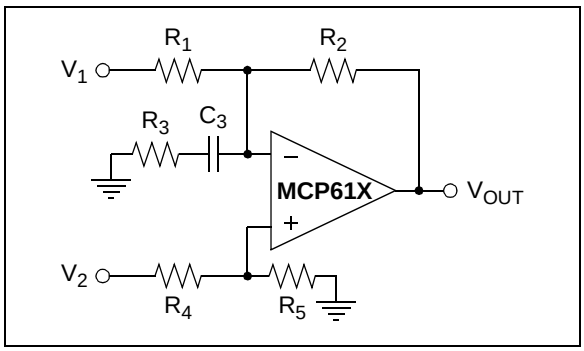


FIGURE 4-2: *Example Circuit for Calculating DC Offset.*

To calculate the DC bias point and DC offset, convert the circuit to its DC equivalent:

- Replace capacitors with open circuits
- Replace inductors with short circuits
- Replace AC voltage sources with short circuits
- Replace AC current sources with open circuits
- Convert DC sources and resistances into their Thevenin equivalent form

The DC equivalent circuit for Figure 4-2 is shown in Figure 4-3.

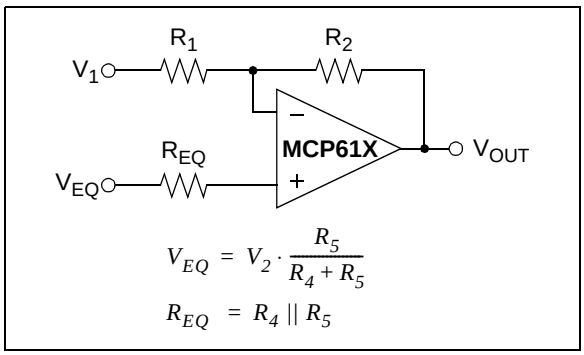


FIGURE 4-3: *Equivalent DC Circuit.*

Now calculate the nominal DC bias point with offset:

EQUATION 4-1:

$$G_N = 1 + R_2/R_1$$

$$V_{OOS} = G_N [V_{OS} + I_B ((R_1 \,||R_2) - R_{EQ}) - I_{OS} ((R_1 \,||R_2) + R_{EQ}) / 2]$$

$$V_{CM} = V_{EQ} - (I_B + I_{OS}/2)\, R_{EQ}$$

$$V_{OUT} = V_{EQ} (G_N) - V_1 (G_N - 1) + V_{OOS}$$

Where:

G_N	=	op amp's noise gain (from the non-inverting input to the output)
V_{OOS}	=	circuit's output offset voltage
V_{OS}	=	op amp's input offset voltage
I_B	=	op amp's input bias current
I_{OS}	=	op amp's input offset current
V_{CM}	=	op amp's common mode input voltage

Use the worst-case specs and source values to determine the worst-case output voltage range and offset for your design. Make sure the common mode input voltage range and output voltage range are not exceeded.

4.3 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP616/7/8/9 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load tied to $V_{DD}/2$. Figure 2-33 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large-signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} conditions in the specification table.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

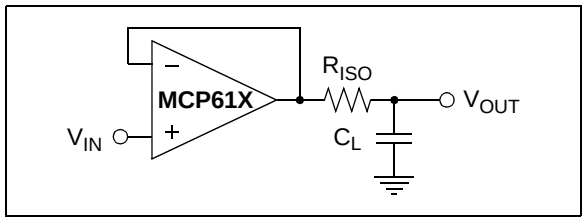


FIGURE 4-4: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-5 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

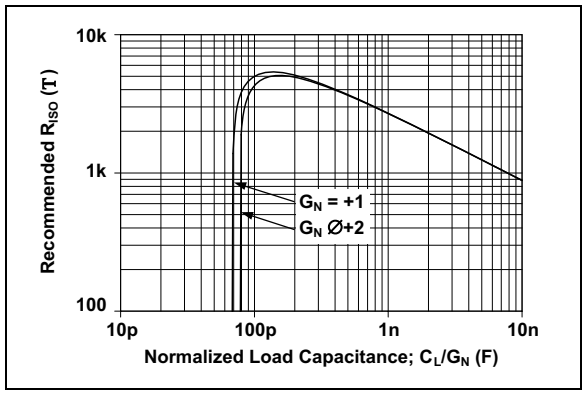


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP616/7/8/9 SPICE macro model are helpful.

4.5 MCP618 Chip Select ($\overline{CS}$)

The MCP618 is a single op amp with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 50 nA (typ.) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier may not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It may use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required and can be shared with other analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP619) should be configured as shown in Figure 4-6. Both circuits prevent the output from toggling and causing crosstalk. Circuit A can use any reference voltage between the supplies, provides a buffered DC voltage and minimizes the supply current draw of the unused op amp. Circuit B minimizes the number of components, but may draw a little more supply current for the unused op amp.

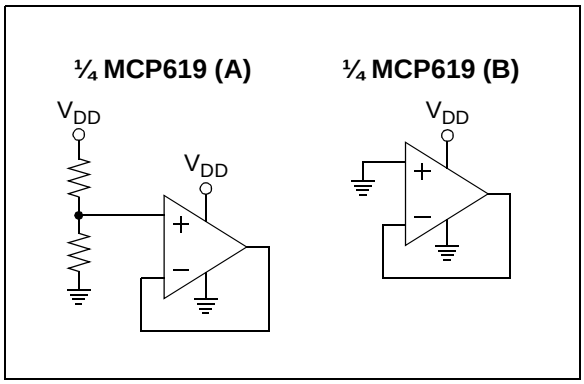


FIGURE 4-6: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP616/7/8/9 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example is shown below in Figure 4-7.

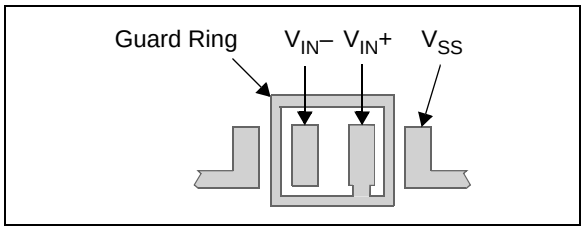


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin ($V_{IN}–$). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin ($V_{IN}–$) to the input with a wire that does not touch the PCB surface.

4.9 Application Circuits

4.9.1 HIGH GAIN PRE-AMPLIFIER

The MCP616/7/8/9 op amps are well suited to amplifying small signals produced by low-impedance sources/sensors. The low offset voltage, low offset current and low noise fit well in this role. Figure 4-8 shows a typical pre-amplifier connected to a low-impedance source (V_S and R_S).

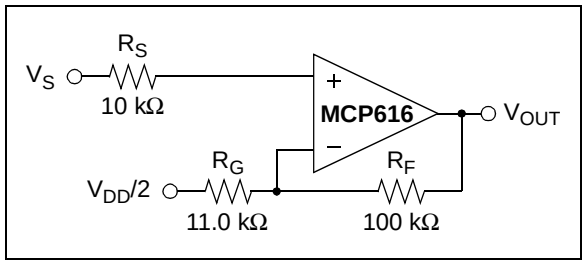


FIGURE 4-8: *High Gain Pre-amplifier.*

For the best noise and offset performance, the source resistance R_S needs to be less than 15 kΩ. The DC resistances at the inputs are equal to minimize the offset voltage caused by the input bias currents (**Section 4.2 "DC Offsets"**). In this circuit, the DC gain is 10 V/V, which will give a typical bandwidth of 19 kHz.

4.9.2 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two-op amp instrumentation amplifier shown in Figure 4-9 serves the function of taking the difference of two input voltages, level-shifting it and gaining it to the output. This configuration is best suited for higher gains (i.e., gain > 3 V/V). The reference voltage (V_{REF}) is typically at mid-supply ($V_{DD}/2$) in a single-supply environment.

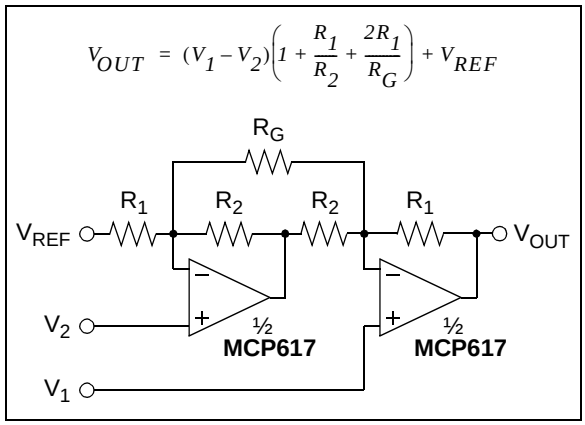


FIGURE 4-9: *Two-Op Amp Instrumentation Amplifier.*

The key specifications that make the MCP616/7/8/9 family appropriate for this application circuit are low input bias current, low offset voltage and high common-mode rejection.

4.9.3 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three-op amp instrumentation amplifier is illustrated in Figure 4-10. The two-input op amps provide differential signal gain and a common mode gain of +1. The output op amp is a difference amplifier, which converts its input signal from differential to a single-ended output; it rejects common mode signals at its input. The gain of this circuit is simply adjusted with one resistor (R_G). The reference voltage (V_{REF}) is typically referenced to mid-supply ($V_{DD}/2$) in single-supply applications.

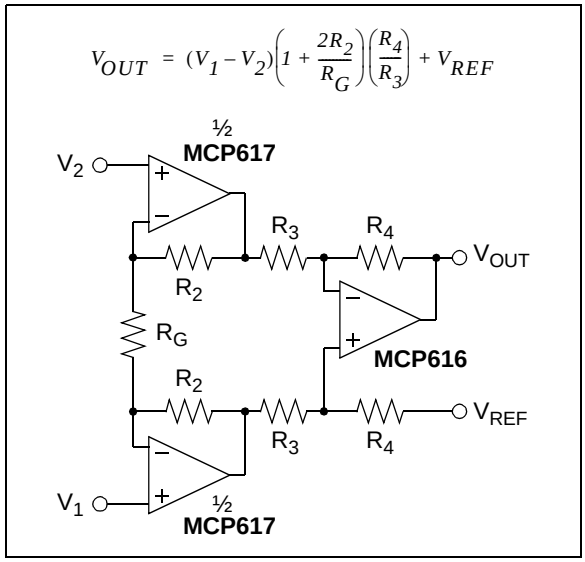


FIGURE 4-10: *Three-Op Amp Instrumentation Amplifier.*

4.9.4 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 4-11, the MCP616 op amp, R_1 and R_2 provide a high gain to the input signal (V_{IN}). The MCP616's low offset voltage makes this an accurate circuit.

The MCP606 is configured as a unity-gain buffer. It isolates the MCP616's output from the load, increasing the high gain stage's precision. Since the MCP606 has a higher output current, and the two amplifiers are housed in separate packages, there is minimal change in the MCP616's offset voltage due to loading effect.

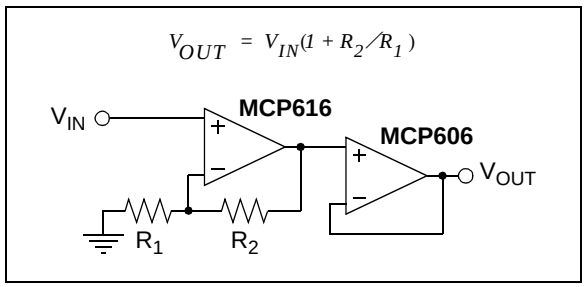


FIGURE 4-11: *Precision Gain with Good Load Isolation.*

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP616/7/8/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP616/7/8/9 op amps is available on Microchip's web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

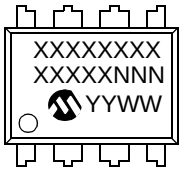
5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative tool that simplifies analog active-filter (using op amps) design. It is available free of charge from our web site at www.microchip.com. The FilterLab software tool provides full schematic diagrams of the filter circuit with component values. It also outpouts the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

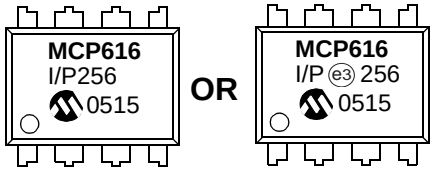
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

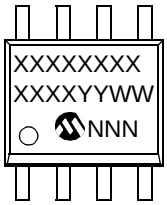
8-Lead PDIP (300 mil)



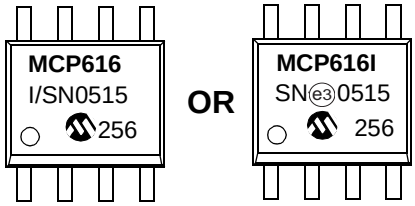
Examples:



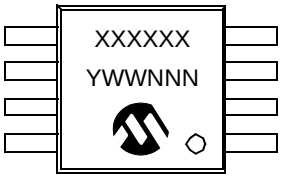
8-Lead SOIC (150 mil)



Examples:



8-Lead MSOP



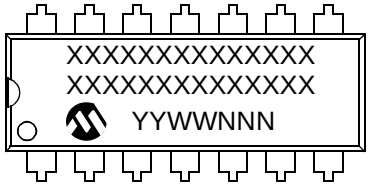
Example:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

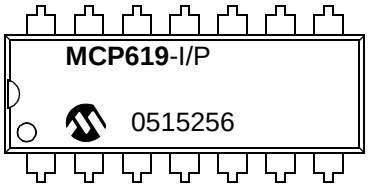
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

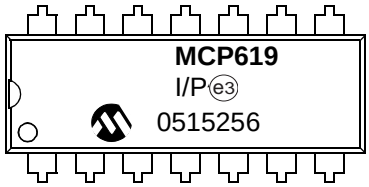
14-Lead PDIP (300 mil) (**MCP619**)



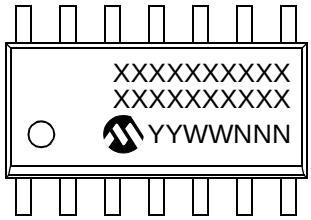
Examples:



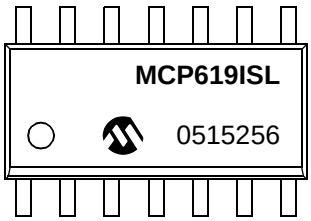
OR



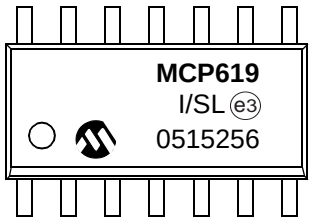
14-Lead SOIC (150 mil) (**MCP619**)



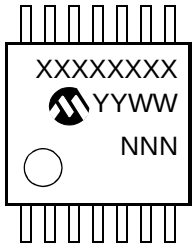
Examples:



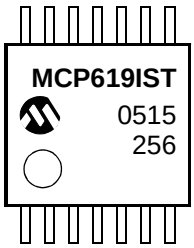
OR



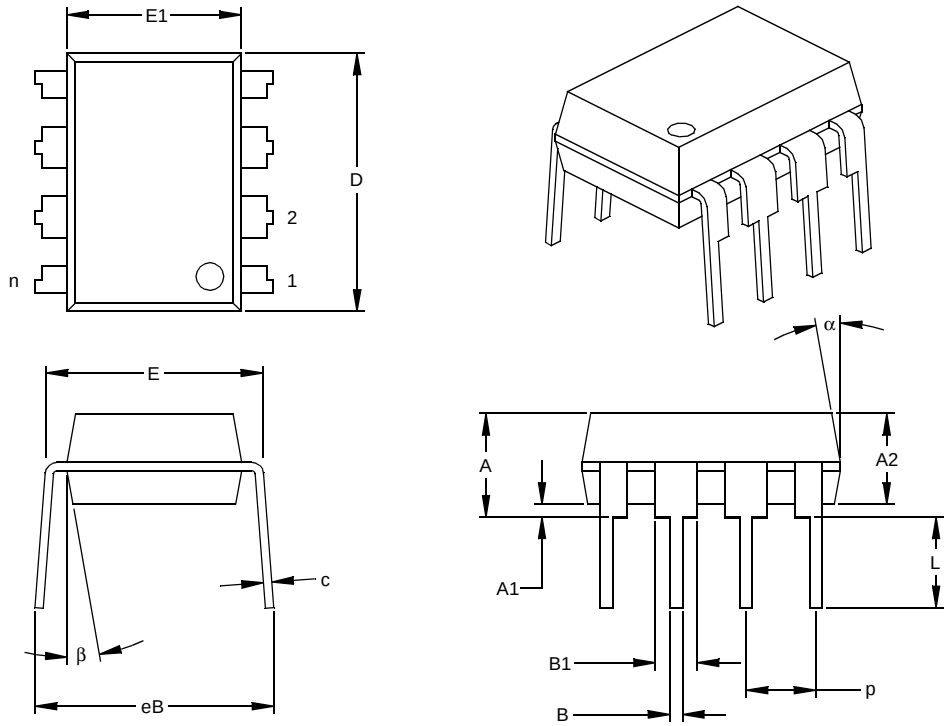
14-Lead TSSOP (**MCP619**)



Example:



8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

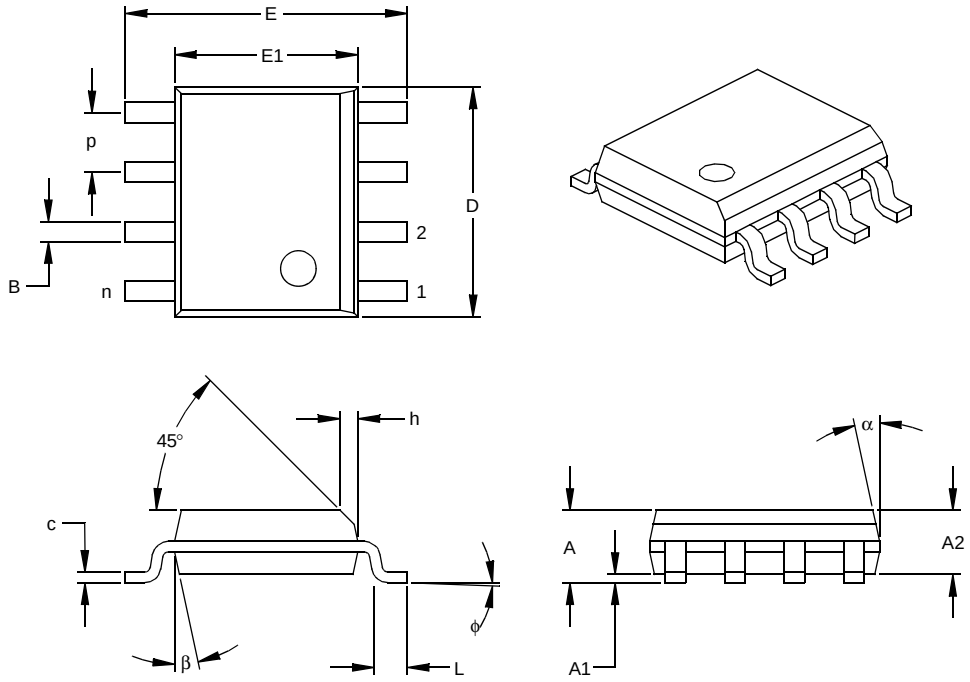


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	a	5	10	15	5	10	15
Mold Draft Angle Bottom	b	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

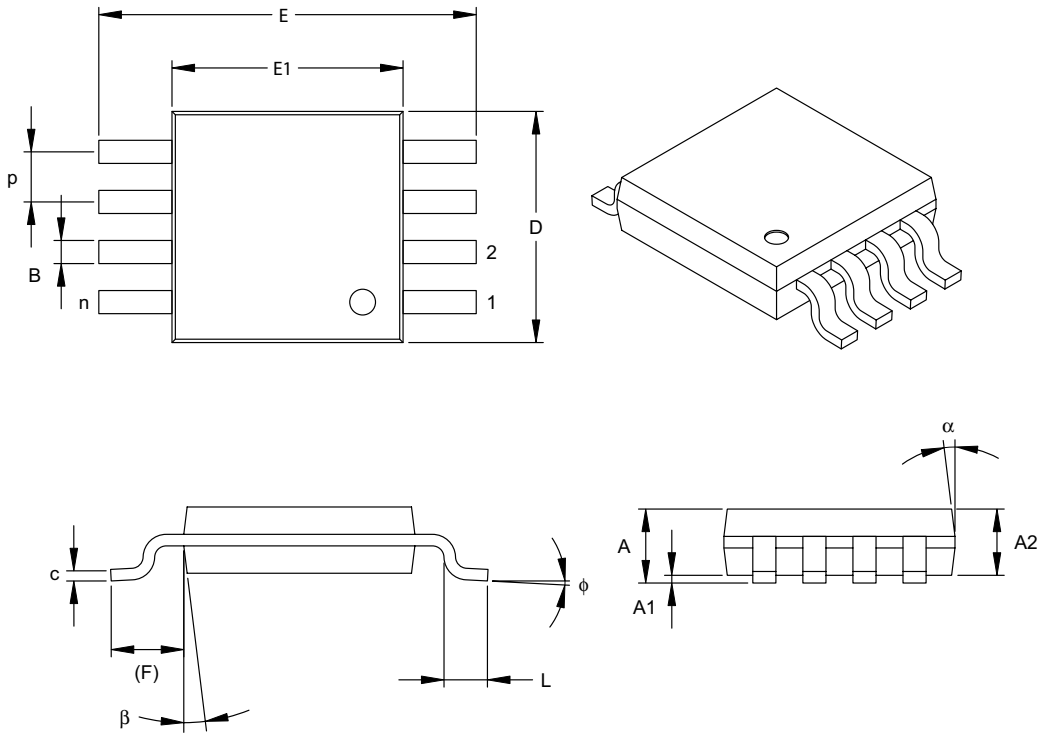


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.026 BSC			0.65 BSC		
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E	.193 TYP.			4.90 BSC		
Molded Package Width	E1	.118 BSC			3.00 BSC		
Overall Length	D	.118 BSC			3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F	.037 REF			0.95 REF		
Foot Angle	ϕ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

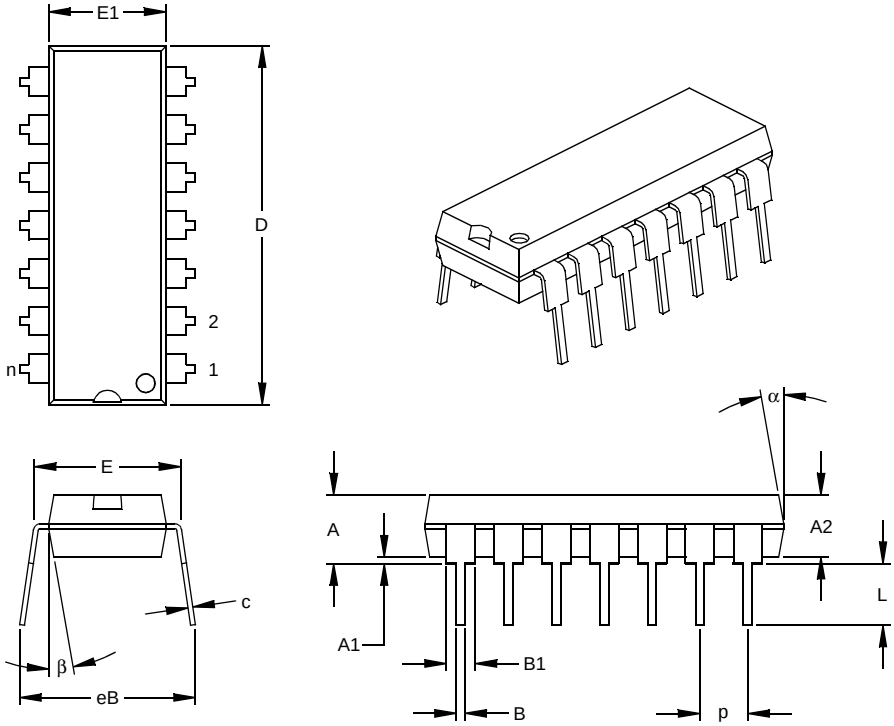
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

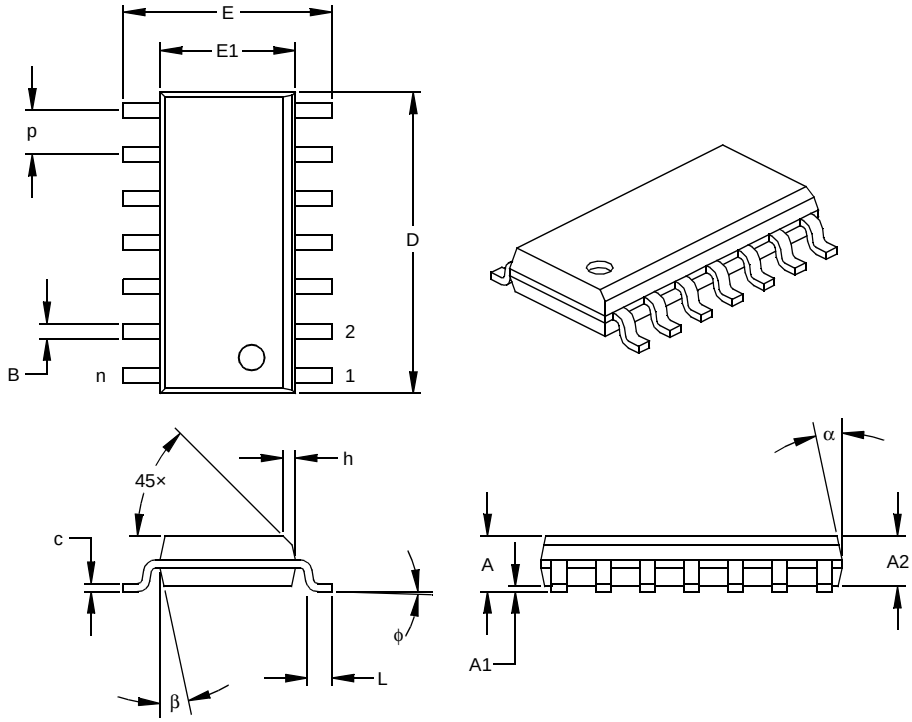


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

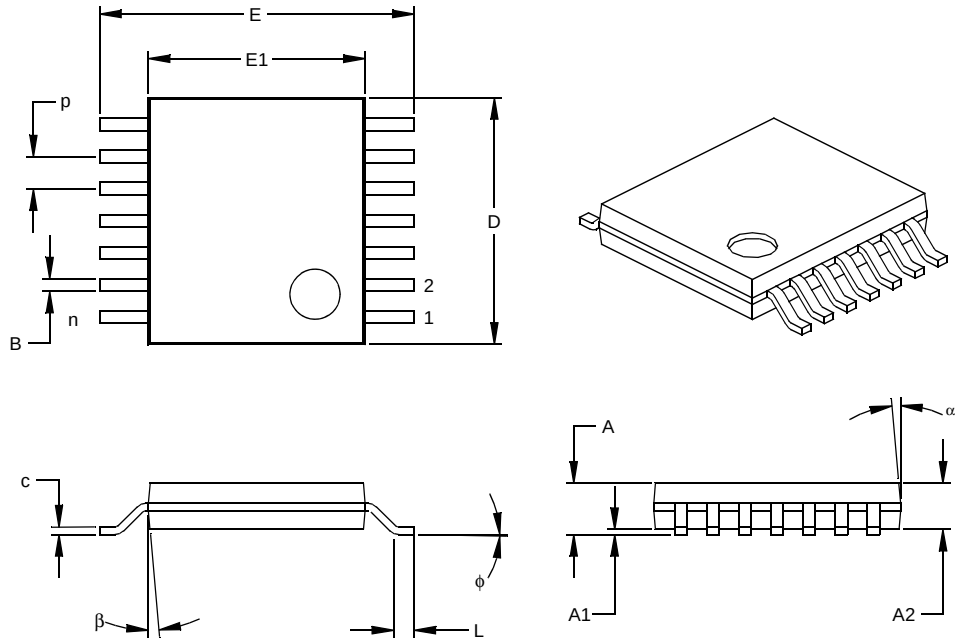


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

APPENDIX A: REVISION HISTORY

Revision B (April 2005)

The following is the list of modifications:

1. Clarified specifications found in **Section 1.0 "Electrical Characteristics"**.
2. Updated **Section 2.0 "Typical Performance Curves"** and added input noise current density plot.
3. Added **Section 3.0 "Pin Descriptions"**.
4. Updated **Section 4.0 "Applications Information"**.
5. Updated the SPICE macro model and added information on the FilterLab software, in **Section 5.0 "Design Tools"**.
6. Corrected package marking information (**Section 6.0 "Packaging Information"**).
7. Added **Appendix A: "Revision History"**.

Revision A (April 2001)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–X	/XX
Device	Temperature Range	Package

Device:	MCP616:	Single Operational Amplifier
	MCP616T:	Single Operational Amplifier (Tape and Reel for SOIC, MSOP)
	MCP617:	Dual Operational Amplifier
	MCP617T:	Dual Operational Amplifier (Tape and Reel for SOIC and MSOP)
	MCP618:	Single Operational Amplifier w/Chip Select (CS)
	MCP618T:	Single Operational Amplifier w/Chip Select (CS) (Tape and Reel for SOIC and MSOP)
	MCP619:	Quad Operational Amplifier
	MCP619T:	Quad Operational Amplifier (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (150 mil Body), 8-lead
	SL =	Plastic SOIC (150 mil Body), 14-lead (MCP619)
	ST =	Plastic TSSOP (4.4mm Body), 14-lead (MCP619)

Examples:

a)	MCP616-I/P:	Industrial Temperature, 8LD PDIP.
b)	MCP616-I/SN:	Industrial Temperature, 8LD SOIC.
c)	MCP616T-I/SN:	Tape and Reel, Industrial Temperature, 8LD SOIC.
a)	MCP617-I/MS:	Industrial Temperature, 8LD MSOP.
b)	MCP617T-I/MS:	Tape and Reel, Industrial Temperature, 8LD MSOP.
c)	MCP617-I/P:	Industrial Temperature, 8LD PDIP.
a)	MCP618-I/SN:	Industrial Temperature, 8LD SOIC.
b)	MCP618T-I/SN:	Tape and Reel, Industrial Temperature, 8LD SOIC.
c)	MCP618-I/P:	Industrial Temperature, 8LD PDIP.
a)	MCP619T-I/SL:	Tape and Reel, Industrial Temperature, 14LD SOIC.
b)	MCP619T-I/ST:	Tape and Reel, Industrial Temperature, 14LD TSSOP.
c)	MCP619-I/P:	Industrial Temperature, 14LD PDIP.

NOTES:

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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