DATA SHEET

BSS92
P-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of April 1995
File under Discrete Semiconductors, SC13b

1997 Jun 19

Philips Semiconductors

PHILIPS

P-channel enhancement mode vertical D-MOS transistor

BSS92

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephony applications
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 (SOT54) variant package.

PINNING - TO-92 (SOT54) variant

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source

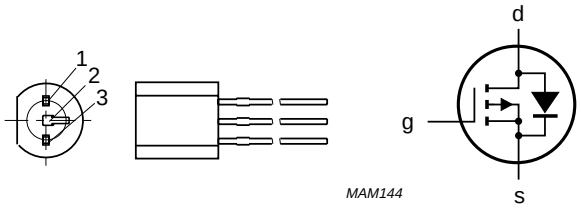


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	–	±20	V
I_D	drain current (DC)		–	–	–150	mA
R_{DSon}	drain-source on-state resistance	I_D = –100 mA; V_{GS} = –10 V	–	10	20	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	–	1	W
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –100 mA	60	200	–	mS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–150	mA
I_{DM}	peak drain current		–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note to the Limiting values and Thermal characteristics

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 10 mm × 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –250 μA	–240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = V_{GS}$; I_D = –1 mA	–0.8	–	–2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –60 V	–	–	–200	nA
		V_{GS} = 0; V_{DS} = –200 V	–	–	–60	μA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –100 mA	–	10	20	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –100 mA	60	200	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	65	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	20	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	6	–	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	–	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	20	–	ns

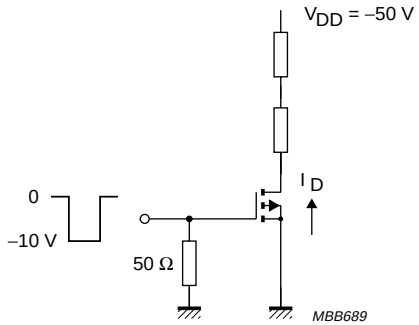


Fig.2 Switching times test circuit.

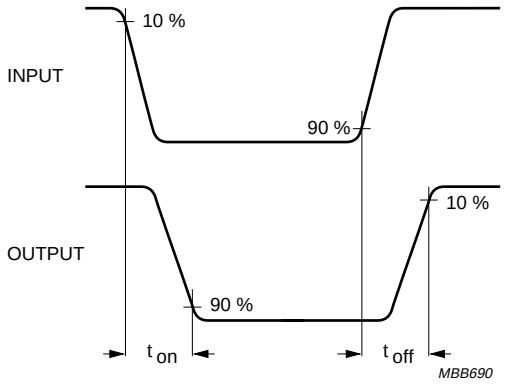
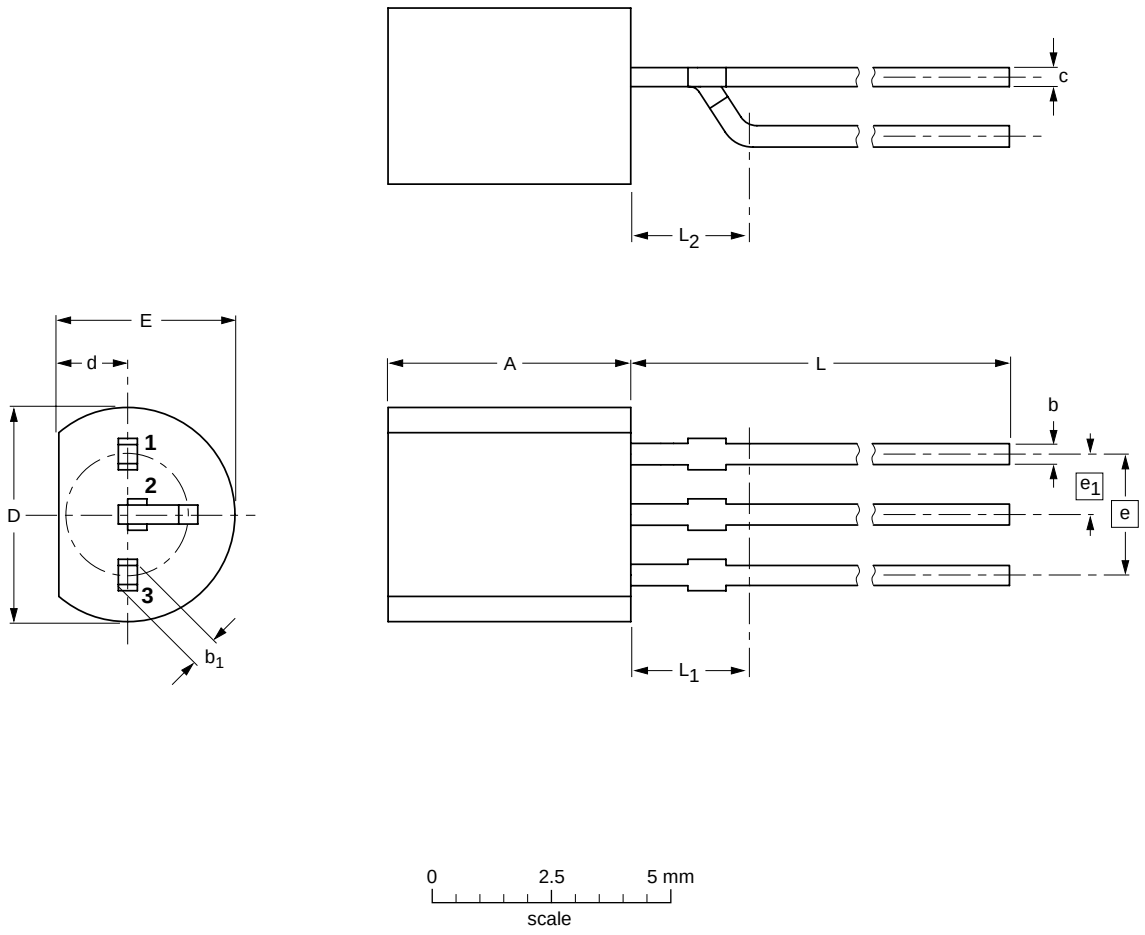


Fig.3 Input and output waveforms.

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92	SC-43			97-04-14